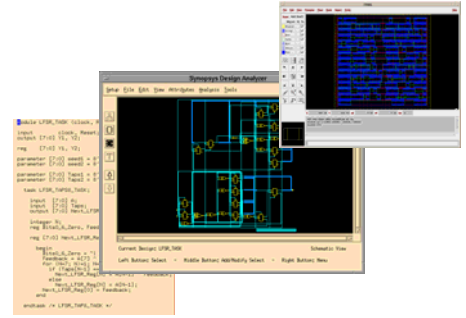


ECE 464, ECE 520 : Digital ASIC Design Spring 2009 Course Overview & Policies



Class Schedule: Monday, Wednesday, Friday 3.50 – 5.05;
EB 2, 1025

Instructor: Professor Paul D. Franzon, Ph.D.
Office: EGRC 443, (919) 515-7351
E-mail: paulf@ncsu.edu
Home page : www.ece.ncsu.edu/erl/faculty/paulf.html
Office Hours: Mon, Wed., Fri 2.30 – 3.30 (EB2 1014 (Lab)). Only on days with scheduled classes. On-campus students are welcome to attend these but I will have an EOL phone-in only office hour 1-2 pm Wed on Wednesdays's with scheduled classes.

Lab TAs/Graders: To be announced on web site.

Class Schedule: Though the schedule is three 75 minute lectures a week, only 29 or fewer lectures will be taught, as per a regular semester. Scheduled classes that will be skipped will be announced each week in advance. You can refer to the class web-site for a detailed schedule.

Communications: Students are strongly encouraged to use the Bulletin Board for questions that are not considered "private". If the question is a good discussion topic, or one that a peer can answer, myself and the TAs might not specifically respond unless it is clear the discussion is not solving it. However, if it is clear that the questions can only be answered by one of us, we will do so as soon as practical. TA-manned Labs should be used for problems related to CAD tool and code debug issues. Though I hold my on-campus office hours in a Lab, my priority will be solving student issues that can not be addressed by a TA. My EOL office hours are telephone, email, Livescribe and (possibly later) Elluminate. For addressing issues that the above methods are not suited for, email is preferred over the telephone.

Labs. Regular TA-manned labs will be established. You will find these very useful for resolving design and tool questions and should be your primary method to do so. EOL students are free to attend labs if they wish. Separate E-labs will be set up for EOL students. Though, as an experiment, I hold my on-campus office hours in a Lab, my priority will be solving student issues that can not be addressed by a TA.

Class Attendance. On campus students are expected to come to class. I will assume that you are up to date on all announcements made in class, and have a copy of all notes provided in the classroom. You are free, however, to use the video classes to review material. . Please bring a copy of the provided notes to class. Though I provide you with an electronic version, you will find it easier to work with a printed version of the notes.

EOL Students. I suggest you use the videos as if they were a class. Print the notes before hand. Add your own notes to them by hand during the lecture.

Textbooks & Notes:

Purchase is Optional.

- M.D. Ciletti, "Advanced Digital Design with the Verilog HDL," (Prentice Hall), 2003. ISBN 0-13-089161-4. This text is a good language guide with numerous examples.
- D.R. Smith and P.D. Franzon, "Verilog Styles for Synthesis," (Pearson Education [Prentice Hall]), 2000. ISBN. 0-201-61860-5. The chapters on design, timing, test benches are lifted straight from this course.
- Course notes, etc. on class web page. **Please make sure you print the first set of notes before the first class.**
- References:
 - Thomas and Moorby, "The Verilog Hardware Description Language", 3rd edition, Kluwer Academic. ISBN 0-7923-9723-1.
 - S. Sutherland, S. Davidman, P. Flake, "System Verilog for Design" (Kluwer), 2004, ISBN 1-4020-7350-8.

- H. Bhatnagar, “Advanced ASIC Chip Synthesis Using Synopsys Design Compiler, Physical Compiler, and PrimeTime”, ISBN 0-7923-7644-7.

You will find the course website and bulletin board on wolfware, as linked from the page www.courses.ncsu.edu/ece520 . I emailed the class earlier week. If you did NOT receive these emails, check your “official” email address at www.ncsu.edu under “directories” in the top right corner, and update it if need be.

Prerequisite: Grade of C or better in ECE 212 or equivalent. ECE 406 is useful but not assumed. Functionally, I assume that students are familiar with logic design, including combinational logic gates, sequential logic gates, timing design, Finite State Machines, etc. If you have never designed and verified even a small digital circuit, and remember the principles by which they work, you will be seriously disadvantaged in this class. I do not assume knowledge of Verilog.

Course Objectives

1. To prepare the student to be an entry-level industrial standard cell ASIC or FPGA designer.
2. To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation, including timing, performance and power optimization, verification and manufacturing test.

Course Outcomes

1. Students will be able to design and synthesize a complex digital functional block, containing over 1,000 gates, using Verilog HDL and Synopsys Design Compiler.
2. Students will demonstrate an understanding of how to optimize the performance, area, and power of a complex digital functional block, and the tradeoffs between these.
3. Students will demonstrate an understanding of issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.

ECE 464 or ECE 520? ECE 520 has wide recognition for preparing ASIC designers for industry. ECE 464 does not. If you are interested in gaining a “job qualification”, and found ECE 406 straightforward, I’ll advise you to take ECE 520, rather than 464. However, the ECE 520 is an order of magnitude more difficult than the 464 project and includes a strong design optimization component. The 464 project does not require much optimization.

Course Approach:

Lectures: Designed to prepare you for the project and cover issues important to ASIC designers.

Laboratories: A lab schedule will be established. Though lab attendance is not required, you are strongly encouraged to use the help available in the labs to sort through homework and project issues. In fact, only minimal help will be available outside the laboratory times.

Homeworks: The homeworks are designed to either help you gain the skills required for the project or to help prepare you for the exams. Collaboration is encouraged though each student is expected to turn in individual solutions.

Project: A fixed project will be published for each class. The project will be done by the students in pairs. You will be evaluated as a pair.

Written Exams : There will be two multiple choice written exams, a one hour midterm and a three hour final. Both are comprehensive, open-book, open-notes exams.

Course Syllabus

1. Introduction to ASIC design
2. Timing design
3. Design of digital hardware using Verilog HDL I
4. Design of digital hardware using Verilog HDL II
5. Design of complex systems. Managing hierarchy.
6. Verification.
7. Design for Test.
8. Low Power Design.
9. Introduction to FPGAs
10. Introduction to SystemVerilog

Homework TurnIn

- On-campus students. Unless specifically requested, please bring a paper copy to class.
- EOL students: Please use online turn in if you can. Otherwise, mail or fax it to the EOL office. The turn-in date is the postmark date, not receipt date.

Student Evaluation

Item	Date	ECE 520	ECE 464
Homeworks		25%	25%
Midterm Exam	February, 20	10%	10%
Project – Prelim Report	March, 10	5%	5%
Project – Final Report	8 am, April 9	40%	40%
Final Exam	Monday, April 27, 1-4 pm	20%	20%

Each non-exam item can be up to one week late with a 10% penalty. After more than a week, the item can not be accepted. Exams are open book, open notes. You may NOT use computers, mobile phones and PDAs during exams. Though you can collaborate during homeworks, **direct copying of solutions, in part or in whole, is not permitted.** All code required for the homeworks should be individually designed and developed. We will be running MOSS on homework solutions, and projects. An Audit requires completing all the homeworks with a grade of at least 80%.

Important Dates

See Calendar

Instructor Research Interests

- Application specific processors. Current projects are in applications of 3DICs and secure IP design.
- Interconnect, including transceivers, electronic packaging, on-chip interconnect, and between-chip interconnect.
- Nanocomputing – how to build the computers that will eventually displace or complement CMOS.

Students with disabilities

Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653. http://www.ncsu.edu/provost/offices/affirm_action/dss/ For more information on NC State's policy on working with students with disabilities, please see http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html

Academic integrity

All the provisions of the [code of academic integrity](#) apply to this course. In addition, it is my understanding and expectation that your submission of any test or assignment means that you neither gave nor received unauthorized aid. **My policy for homeworks and projects is that while you are free to collaborate, sharing of design data, specifically Verilog code, is expressly forbidden. If you collaborate on a design problem, I still expect you to turn in individually developed code.**