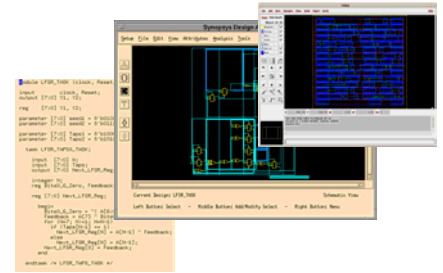


ECE 406: Design of Complex Digital Systems Fall 2002 Course Overview & Policies



Class Schedule: Tuesday, Thursday, 4:30 – 5:45, Daniels 429

Instructor: Professor Paul D. Franzon, Ph.D.
Office: EGRC 443, 515-7351
E-mail: paulf@ncsu.edu
Office Hours: Tue 3.00 – 4.00/Thur 6.00-7.00 (in DAN 307)

Lab TA/Graders: To be announced. Due to the size of this class, please use the wolfware bulletin board and the TAs as your first point of contact to resolve lab and HW questions.

Textbooks & Notes: The recommended text for this course are:

- “Verilog Styles for Synthesis of Digital Systems”, David R. Smith and Paul D. Franzon, Prentice Hall, ISBN 0-201-61860-5

The following books may be useful and are on reserve in the Library.

- “Verilog HDL Reference Guide”, Sutherland HDL Consulting (*This is very useful*).
- “Computer Organization and Design: The Hardware/Software Interface”, Hennessy and Paterson, Morgan Kaufman, ISBN 1-55860-281-X (*Explains the MIPS ISA*)
- “Verilog HDL”, Samir Palnitkar, SunSoft Press, ISBN 0-13-451675-3.
- “HDL Chip Design”, D.J. Smith, Doone, ISBN 0-9651943-3-8. (*This is a really good book if you plan to be a professional in this RTL-based hardware design.*)
- “The Verilog Hardware Description Language”, 3rd edition, Thomas and Moorby, Kluwer Academic Press, ISBN 0-7923-9723-1.
- “Logic Synthesis Using Synopsis”, Kurup and Abbasi, Kluwer Academic Press, ISBN 0-7923-9582-4.
- “MIPS RISC Architecture”, G. Kane, Prentice Hall, ISBN 0-13-584749-4.
- “Verilog Quickstart”, J.M. Lee, Kluwer Academic Press, ISBN 0-7923-9927-7.

Course notes, homework and lab assignments, etc.: Some of these will be distributed as handouts and some made available in the wolfware course. ***Please make sure that you print the first set of notes before the first class from the website.*** Also note that the notes distributed on-line are NOT the complete notes for the class. Classroom attendance and note-taking is expected.

Class Locker: <http://www.courses.ncsu.edu/ece406/>

Prerequisite: Grade of C or better in ECE 206 or equivalent.

Course Objective: A study of techniques for design of digital systems. Design of system modules from functional and interface specifications will be studied. A progression of designs culminating in the design of a digital processing unit (CPU) will be used to illustrate these techniques. This course will utilize a modern Hardware Design Language (Verilog) for the design of digital modules. While implementation at the logic component level will be briefly studied, the focus will be on system-level design. Design of microprogrammed digital systems and module interfacing schemes will also be discussed.

Homework: Assignments will be issued regularly (~ every other week).

Laboratory Assignments: The laboratory projects are an integral part of the course and are intended to provide experience in the application of the design techniques discussed in lecture. These projects will utilize the Cadence suite of design tools to design and simulate operation of digital modules.

Laboratory Schedule: There are several laboratory times scheduled. All students must be registered for one of these time slots. Workstations in Daniels 242 will be reserved for your use and lab TA's will be available to assist you during those times. You will be free to work on your lab projects at times of your convenience. However, if you wish to work when the TA's are available, students registered for that particular time slot will have priority.

Collaboration: For homework and laboratory projects, though collaboration is sanctioned (and encouraged), direct copying is not and students must turn in individual submissions. Realize that mastery of the material in the homework and lab assignments will be essential for a good performance on the exams!

Lecture Plan: The lectures will generally follow the order of the list of topics below; however, schedules and topics are subject to change.

1. Introduction to digital systems
2. The Verilog Hardware Description Language and its use in digital design
3. Finite State Machines
4. Digital sub-system building blocks
5. Designing a MIPS CPU

Exams: There will be two 75-minute in-class exams and a comprehensive final exam. Exams will be open book / open notes and multiple choice. As a general policy, make-up exams will not be given. The mid-terms will be cumulative, while the final will be comprehensive. If you have a conflict with a scheduled exam, you must notify me in advance to arrange an alternative. Likewise, if you are unable to take an exam due to illness or emergency, you must notify me immediately.

Grading:	Homework	15%	(1)
	Laboratory	25%	(2,3)
	Exam #1	15%	September 19 (tentative date)
	Exam #2	15%	October 31 (tentative date)
	Final Exam	30%	December 12, 1:00 PM

Grading Notes:

1. Homework assignments will not be accepted after solutions are posted or distributed.
2. Laboratory reports turned in late will be assessed an automatic penalty of 10%. Reports turned in more than 1 week late will be assessed a 25% penalty.
3. All laboratory projects must be completed with a minimum grade of 50% each to earn a C or better.

Important Dates

- Classes August 20 – December 5, except October 15, November 28, and other announced dates.
- Last date to drop : September 30.