

## ECE 733 Homework 1

**Make a one page summary of your answers and turn them in with your homework as the first page. (Use template on last page).**

### Question 1

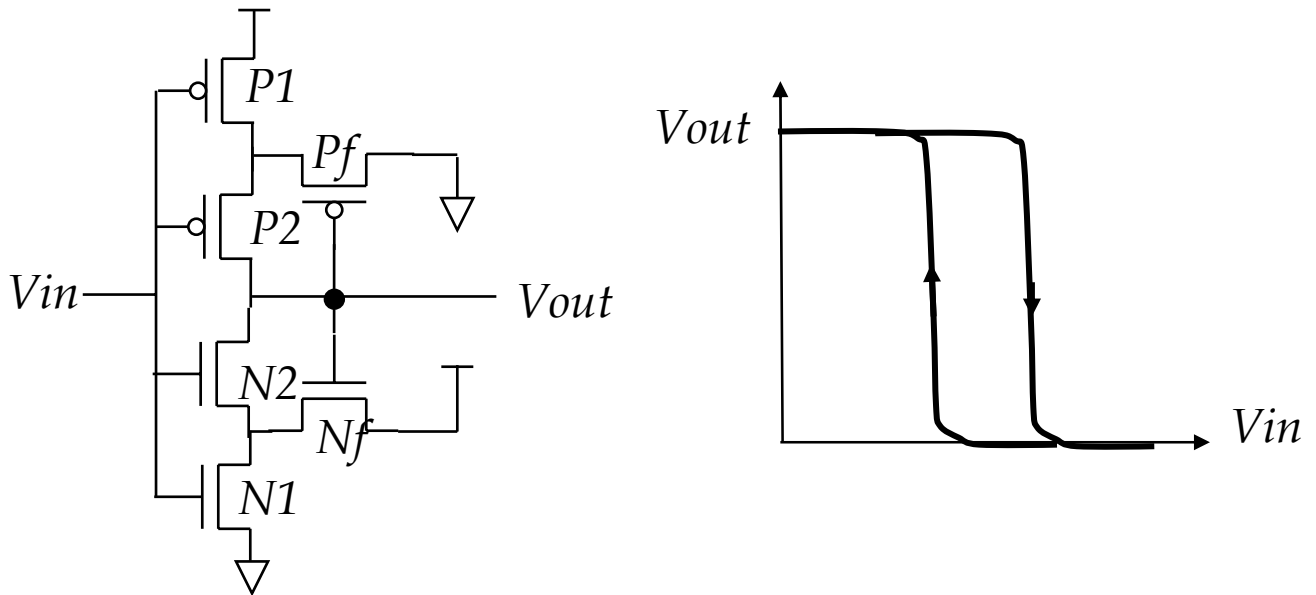
This is a straightforward revision question.

Design a static gate that performs  $F = ((A+C).(B+D))'$ . [10 points]

### Question 2

This is a more complex revision question that forces you to think through the operation of a more complex static gate and revisit the first level device equations.

Consider the Schmitt Trigger gate. This is useful at noisy inputs as it provides an improved noise margin.



Obtain approximate expressions for  $V_{IL}$  and  $V_{IH}$  in terms of  $k_{Nf}$ ,  $k_{N1}$ , etc. Use the first order transistor equations and ignore the body effect. Note that normally  $N_f$  and  $P_f$  are larger than the other transistors. [20 points]

Hint : Estimate  $V_{IH}$  by determining the smallest  $V_{in}$  that permits transistor N2 to turn on. What states are  $N_f$  and  $N1$  in when N2 just turns on? Equate these currents (as N2 is just on), and that will give you  $V_{DS\_N1}$ . You can then calculate  $V_{in}$  that just turns N2 on. Estimate  $V_{IL}$  by determining the  $V_{in}$  that turns P2 on, while  $V_{in}$  is rising.

### Question 3

The main purpose of this question is to get you to start using Spice and to perform some of the trade-off analyses typical for this class. Please note the following:

- Use the 45 nm technology files that were used in ECE 546 in Fall 2008.
- I prefer you use Cadence Composer for schematic capture, rather than write a Spice Netlist by hand. That way, I know you have the drain and source areas and perimeters correct. If you are doing the Spice Netlist by hand, make sure to check these figures.
- Make sure to use the power calculation approach outlined on the CAD tool tips (resources) page.

Design a Schmitt Trigger gate so that  $NMH = NML$  within a range of 10%. Make sure the design works in simulation to this specification. When loaded with a minimum size inverter (both nfet and pfet at minimum size) what is the gate delay (use an input waveform with a 0-100% rise time of 100 ps)? Measure the average power consumption over an interval of 5 ns with the following conditions:

- Input: Low for 1 ns. 100 ps rising edge (0 to 100% rise time). High for 2 ns. 100 ps falling edge (100% to 0% fall time).
- Loaded with a CMOS inverter containing minimum size gates. Do not include the power consumption of the CMOS inverter in the power figure.

Report your results, including the schematic and plots of corresponding delay waveforms.

**Name:**

**Student ID:**

**Q1. Schematic**

**Q2.  $V_{IH}$ =**

**$V_{IL}$ =**

**Q3. Power Consumption =**

**Gate Delay =**

Sketch design, including transistor sizes.

If you need revision on the concepts assumed as background for this course then I suggest the following reading:

Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”

Ch.1. gives you an overall perspective. Completes your background.

Ch. 2. Though I briefly revise it, I assume you are familiar with the main modes of operation of the MOSFET and the governing equations. Linear, Saturation regions.

Ch. 4. The first four sections (through to wiring) are very important, especially transistor sizing. The other sections are good background. Even if you have ECE 511, please review this.

Ch. 5. You will be making heavy use of Spice.

Ch. 6. All the circuit families sections (first five sections) are very important. Again, please review this even if you have ECE 511.

Ch. 7. The first few sections up to and including “circuit design of latches and flip-flops”. Again, please review this even if you have ECE 511.

Go to [www.eda.ncsu.edu](http://www.eda.ncsu.edu) and DO the first listed tutorial “Analog Artist with HSpice”. This refers to the freepdk45 library that you are to use in the rest of this class.

All on-campus students are expected to use Analog Artist. I would encourage EOL students to use Analog Artist but I understand that it sometimes does not work well remotely. Hspice can be used through a textual interface. It is a little tedious but quite workable. We will get a brief tutorial together for you and I could delay HW1 due date if this affects you.