

ECE 733 Project 2

Due : Friday, April 24, 2009 in class
(Up to one week late with a 10% penalty.)

On campus project: Transceiver Design

(Off campus, section 601, students can do this project if they elect to do so.)

Design a 1-bit wide 45 nm differential transceiver that meets the following constraints and goal:

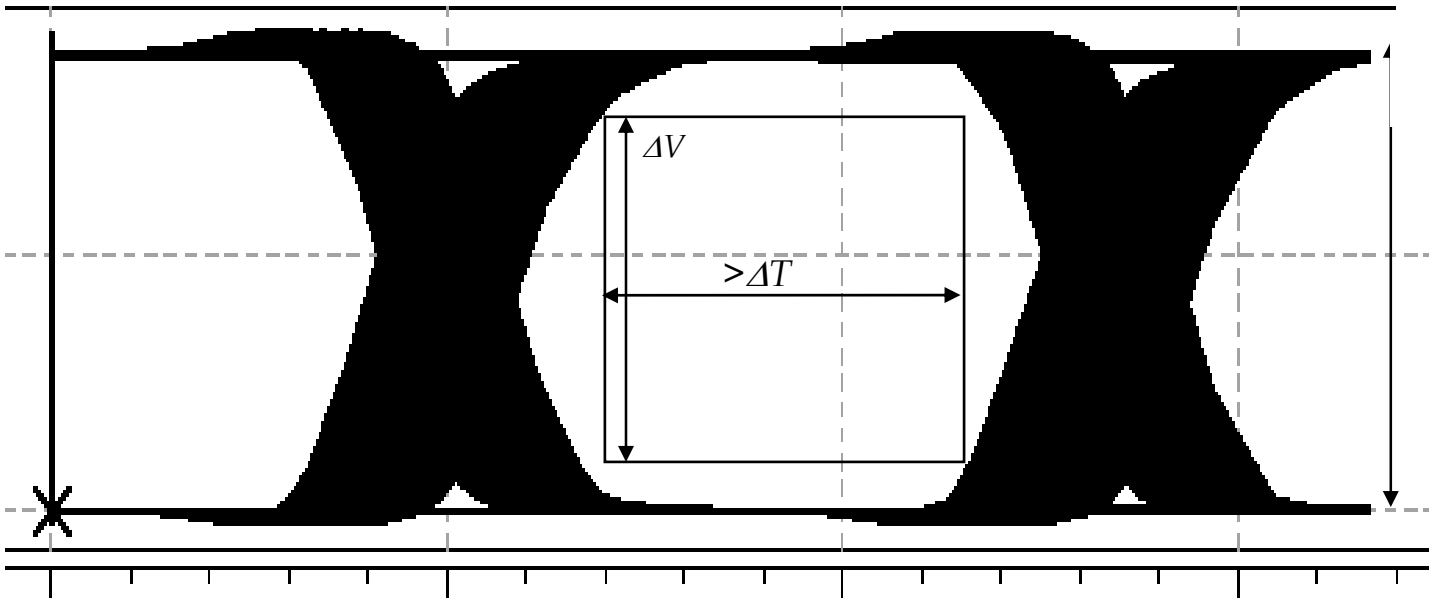
- Operating over a 100 cm long lossy differential transmission line, with 0.25 pF of load capacitance added at each end (to represent pad capacitance).
- Operating at an actual data rate of at least 4.0 Gbps while meeting the template on the next page for a BER of better than 10^{-12} .
- Your design GOAL is to minimize the metric **energy*BER** for the data sequence below. Your power must include all components in your design except for your flip-flops. You are to assume that each flip-flop has a average power consumption of 80 μ W at 4 Gbps.
- You should reuse your flip-flop from project 1 but replace its power consumption with 80 μ W. (The purpose for this is to not reward you twice for a low power project 1 result.) Note, you have to modify the output to make it as close to being purely differential as you can. i.e. Q and Qbar must be as close together in time as possible. Please do not add in the power of this circuit to your measured power. (Note, this is why the bit rate here is slower than project 1 – to allow for this circuit).
- Use the device Spice Models from project 1
- While meeting an eye specification of an eye aperture opening, measured by the Cscope tool, specified below (as measured at the final output of your RX BEFORE data recovery) while executing the following 128-bit sequence (the gaps are to add readability):
 - 0101 1001 0100 1100 0001 0000 0101 1111 0111 1100 0101 0001 1100 0011 1101 0101 REPEATED TWICE
 - Note: The maximum run length in this sequence is 5 bits. I ask for a 128 bit sequence so as to ensure plenty of opportunities for ISI due to reflection noise.
 - You can use the “.include” feature in Hspice to read in a data file generated elsewhere.
- You have data complementary inputs operating at 4 Gbps.
- Correct transistor perimeter and area parameters must be included in the spice netlist.
- Ideal voltage and current sources cannot be used to supply biases to internal circuitry. However, ideal spice implementations can be used for bandgap reference and OpAmp designs if used.
- All clocks must be buffered by an inverter so as to give a reasonable rise time. (You can resize the transistors in this pair.) THIS INVERTER IS TO BE INCLUDED IN YOUR POWER CONSUMPTION.
- All inputs should have rise and fall times of 30 ps.

- Use the differential circuit structure, with resistor compensation, as defined in the class notes.
- The load at EACH end of each transmission line is to be 0.25 pF (representing pads, package, etc.)
- Temperature = 90 C

Otherwise, you are free to use any technique you see fit, including differential circuits, equalization, termination, coding, etc. (Note if you use coding, you must report the effective data rate, and achieve at least 4 Gbps in that rate, not the coded rate).

Required Eye Opening at final RX output

You must achieve the following eye opening at the RX output, before any resynchronization flip-flop. This is a differential eye.



The eye diagram versus Bit Error Rate (BER) tradeoff is summarized in the following table:

ΔV	ΔT	BER
400 mV	0.9 UI	$2 \cdot 10^{-13}$
300 mV	0.85 UI	$5 \cdot 10^{-13}$
200 mV	0.8 UI	10^{-12}

This is measured at the RX input.

Deliverables

A report describing the approach used, including circuit topology, design procedure, simulation results, and achieved speed. All results should be presented in the **body** of the report (in tables if possible). Relevant schematics, plots, netlists, text files, etc. should be clearly referenced and included in the appendix. Binary text files do not need to be included.

- It is important to document your design procedure.
- **Please include an eye diagram, showing the points that lie outside of the template above for your claimed ΔV and ΔT .**

Evaluation

You will be evaluated out of 100 and assigned a grade based on the following criteria:

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You will be evaluated out of 100 and assigned a grade based on the following criteria:

80 : This is the grade that will be given to a basic, working complete project. I.e. If it meets the constraints described above.

70-79 : Missing one or two major attributes above. E.g. Being slower.

0-69 : A submission that clearly does not achieve the goals established here. E.g. Does not work, very slow maximum speed.

10 additional points are allocated for the quality of the report. This brings the base grade up to 90.

Up to 15 bonus points are earned competitively based on power consumption, EXCEPT FOR THE FLIP-FLOPS. The worst power will earn 0 points, the best 15, and those in between will get bonus points on a linear scale. Note, you can earn 105 points for this project.

Collaboration

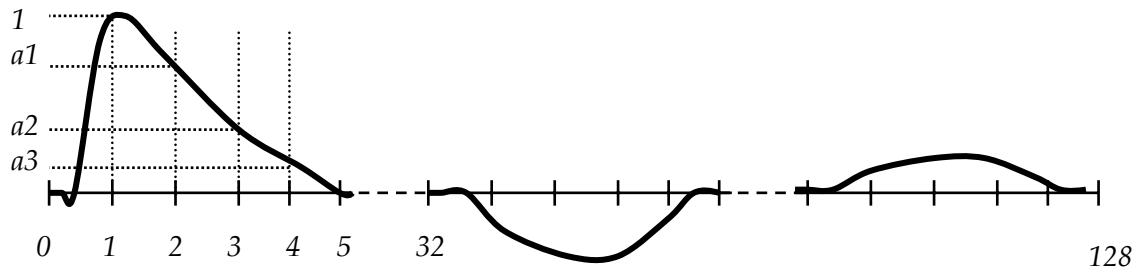
If you help each other that is fine, in fact encouraged. However, I expect that each of you do your own design, design capture, optimization, simulations and

interpretation for the final report. I further expect each design to be unique, at least on the details of transistor sizes. If it is clear that someone rode completely on another student's work, both students will be penalized. I request that you DO NOT share electronic versions of your designs or results. E.g. Explaining, in detail, how your design works to a friend is good, emailing that friend your schematic file is very bad and, if discovered, will be considered an academic violation.

Recommended Design Procedure

Step 1. Termination and equalization design.

The main tool in reducing ISI is analyzing the pulse response of the circuit. Take the Tline model given in the accompanying Spice file, add in the 0.25 pF of capacitance at each end, and design a suitable single stage differential amplifier TX and RX. Apply a 010 pulse at the driver and observe the time domain response at the RX. Observe the pulse response for at least 128 bit periods, so you have a chance of seeing reflection noise. You should see a pulse response something like this (note I have normalized the 010 swing at the RX for the bit pulse to be 1):



The bumps that are many bits out are due to reflection and the tail-end of the initial pulse response is due to the channel response. You should eliminate those first by using appropriate terminations. Options include terminating at one end only or both ends, terminating just the differential mode or both the DM and CMs. Note, I gave no common mode requirements on the input eye; the RX has good common mode rejection.

Resimulate after you have decided on the appropriate termination. You now have to design equalizer. You can take a first stab at the equalizer by looking at the ISI following 1 UI (UI's 2, 3, and 4 here). The role of the equalizer is simply to reduce this ISI to acceptable levels. The easiest way to do this is simply to subtract out the expected ISI by using the following filter:

$$1 - a_1 z^{-1} - a_2 z^{-2} - a_3 z^{-3}$$

Etc. Note here I use a 3-tap filter. You might desire more or fewer taps depending on the ISI that you see.

You should then implement this filter in Spice, using perfect sources and check the pulse response has minimal ISI.

Alternatively, you can design the filter in the frequency domain if you wish. The objective is a flat band pass and linear phase response over the frequency content of the data.

Step 2. Circuit Design

Now implement a driver circuit that satisfies this bandwidth, swing and eye opening specified above. In your report describe the initial design of the circuit and how you traded off swing, bandwidth, and power. Describe how you biased and sized the current mirrors and reference circuit, and any other circuits you use. Clearly show how the Spice simulation that resulted from your initial design was used to guide the steps towards the final design.

Optional 601 section project

(This project is not available to on-campus students).

Write an insightful review on progress and challenges regarding future high-speed SERDES, with a specific emphasis on a multilevel signaling scheme, such as PAM-4 or duobinary. Focus on one or a few aspects, rather than giving the topic a broad-brush review. Examples of aspects include circuits to support these schemes, BER and power tradeoffs, comparisons with PAM-2, unique challenges yet to be solved. Two references have been placed in the password protected area of the class website but you are encouraged to explore further on your own (you have access to IEEE explorer at the library web page).

Your report should be two to four pages long in 11 point font. Grading criteria to be applied include the following:

- Insightfulness of review. Did you penetrate to the core issues? Does the review concisely present important topics in a useful way?
- Thoroughness of investigation. Did you conduct a full investigation, or is it just a cursory summary?
- Organization, grammar and spelling. Is it readable and easy to follow?

Two possible starting references are:

- Zerbe et.al., “Equalization and clock recovery for a 2.5 – 10 Gbps 2-PAM/4-PAM Backplane Transceiver Cell”, IEEE JSSC 38(12), December 2003, pp.2121-2130.
- Stojanovic, et.al., “Autonomous Dual-Mode (PAM2/4) Serial Link Transceiver with Adaptive Equalization and Data Recovery”, IEEE JSSC 40(4), April 2005, pp. 1012-1026.

Background References

- [1] W. J. Dally and J. Poulton, "Transmitter equalization for 4Gb/s signaling", *IEEE Micro*, vol17, issue1,Jan.-Feb. 1997.
- [2] Mark Horowitz, C.-K. Ken Yang and Stefanos Sidiropoulos, "High-Speed Electrical Signaling: Overview and Limitations", *IEEE Micro*, Volume: 18 , Pages:12-24 , Jan.-Feb. 1998
- [3] C.-K. K.Yang et al., "A 0.5 μ m CMOS 4.0-Gbit/s Serial Link Transceiver with Data Recovery Using Oversampling", *IEEE J. Solid-State Circuits*, vol. 33, NO. 5, May 1998.
- [4] M. J. E. Lee, W. J. Dally and P. Chiang, "Low-power and efficient high speed I/O circuit techniques", *IEEE J. Solid-State Circuits*, vol. 35, pp. 1591-1599, Nov 2000.
- [5] R. Farjad-Rad et al., "0.622-8.0 Gbps 150mW serial IO macrocell with fully flexible preemphasis and equalization," *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, June 2003, pp. 63-66.
- [6] V. Stojanovic, A. Ho, B. Garlepp, F. Chen, J. Wei, E. Alon, C. Werner, J. Zerbe, M. A. Horowitz, "Adaptive equalization and data recovery in a dual-mode (PAM2/4) serial link transceiver", *Digest of Technical Papers on VLSI Circuits*, pp348-351, June 2004.
- [7] J. Montanaro, et al., "A 160-MHz 32-b 0.5-W CMOS RISC microprocessor," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1703-1714, Nov. 1996.
- [8] S.Sidiropoulos and M. A.Horowitz, "A semidigital dual delay locked loop," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1683-1692, Nov. 1997.
- [9] Jeongsik Yang, et al., "A Quad-Channel 3.125Gb/s/ch Serial-Link Transceiver with Mixed-Mode Adaptive Equalizer in 0.18 μ m CMOS," *ISSCC 2004 Digest of Technical Papers*, pp176-177, Feb.2004
- [10] J. Cao, et al., "OC-192 Transmitter and Receiver in Standard 0.18 μ m CMOS", *IEEE J. Solide State Circuits*, vol. 37, no. 12, pp. 1768-1780, Dec. 2002
- [11] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate linear phase detector," *IEEE J. Solid-State Circuits*, vol. 36, pp. 761-767, May 2001.
- [12] Famin Farjad-Rad et al., "A 33mW 8Gb/s CMOS Clock Multiplier and CDR for Highly Integrated I/Os", *IEEE J. Solid-State Circuits*, vol. 39, pp1553-1561, Sep 2004.
- [13] Hiok-Tiaq Ng et al., "A second order semidigital clock recovery circuit based on injection locking", *IEEE J. Solid-State Circuits*, vol. 38, pp2101-2110, Dec 2003.
- [14] Garlepp et al, "A portable digital DLL for high-speed CMOS interface circuits", *IEEE J. Solid-State Circuits*, vol 33, pp632-644, May 1999.

Text portion is limited to FOUR ages, 12 point font, 1” margins. Use additional pages for figures as needed.

Title, Name

Abstract. Summarize key results. E.g. “This report describes ...”

1. Introduction

Introduce purpose of project, and outline of report. Your target audience is a potential employer, not a project evaluator.

2. Technical Approach

Describe how you approached the design and iterated on it until you obtained the desired results.

3. Key Simulation results

Show annotated simulation results clearly supporting claimed timing and power numbers.

4. Conclusions

Brief conclusions describing what was achieved and any unique features demonstrated.

Table 1:

Parameter	Horizontal Eye	Vertical Eye	Power
TX/RX			

Figure 1. Eye Diagram. Mark required template clearly on waveforms.

Figure 2. Pulse response before equalization, showing tap weight calculation.

Figure 3. Final Schematic (full page). Transistor sizes clearly readable.

Figure 4. Pulse response after equalization.

Other figures can be included as needed.

Appendices

Spice Netlist (pages as needed)

Result File (.mt0)

Plot of power consumption