

**ECE 733: Digital Electronics**  
**Spring 2009**  
**Course Overview & Policies**

**Class Schedule:** Monday, Wednesday, Friday, 5.20 – 6.35 EB2 1230

**Instructor:** Professor Paul D. Franzon, Ph.D.  
 Office: EGRC 443, (919) 515-7351  
 E-mail: paulf@ncsu.edu

Home page : [www.ece.ncsu.edu/erl/faculty/paulf.html](http://www.ece.ncsu.edu/erl/faculty/paulf.html)

Office Hours: Mon, Wed., Fri 2.30 – 3. 30 (EB2 1014 (Lab)). Only on days with scheduled classes. On-campus students are welcome to attend these but I will have an EOL phone-in only office hour 1-2 pm Wed on Wednesdays's with scheduled classes.

**Lab TA/Graders:** Announced on web site.

**Class Schedule:** Though the schedule is three 75 minute lectures a week, only 32 or fewer lectures will be taught, as per a regular semester. Scheduled classes that will be skipped will be announced each week in advance. You can refer to the class web-site for a detailed schedule.

**Communications:** Students are strongly encouraged to use the Bulletin Board for questions that are not considered “private”. If the question is a good discussion topic, or one that a peer can answer, myself and the TAs might not specifically respond unless it is clear the discussion is not solving it. However, if it is clear that the questions can only be answered by one of us, we will do so as soon as practical. TA-manned Labs should be used for problems related to CAD tool and code debug issues. Though I hold my on-campus office hours in a Lab, my priority will be solving student issues that can not be addressed by a TA. My EOL office hours are telephone, email, Livescribe and (possibly later) Elluminate. For addressing issues that the above methods are not suited for, email is preferred over the telephone.

**Labs.** Regular TA-manned labs will be established. You will find these very useful for resolving design and tool questions and should be your primary method to do so. EOL students are free to attend labs if they wish. Separate E-labs will be set up for EOL students. Though, as an experiment, I hold my on-campus office hours in a Lab, my priority will be solving student issues that can not be addressed by a TA.

**Class Attendance.** I prefer that on campus students to come to class. However, this year, the video lectures are recordings of the actual class, so if you prefer an on-line format, that is acceptable to me. Please bring a copy of the provided notes to class. Though I provide you with an electronic version, you will find it easier to work with a printed version of the notes.

**EOL Students.** I suggest you use the videos as if they were a class. Print the notes before hand. Add your own notes to them by hand during the lecture.

**Textbooks & Notes:**

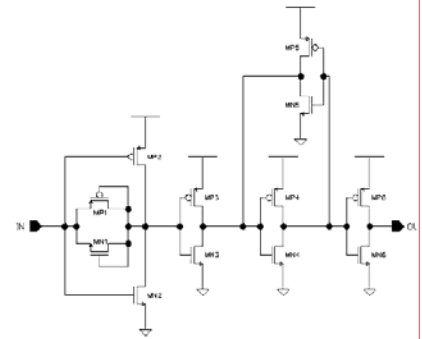
Purchase is optional:

- K. Bernstein, et.al., “High speed CMOS Design Styles,” Kluwer, ISBN 0-7923-8220-X

References

- S-N Kang, and Y. Leblecici, CMOS Digital Integrated Circuits, ISBN 0-07-038046-5
- R.X. Gu, K.M. Sharaf, M.I. Elmasry, High Performance Digital VLSI Circuit Design, ISBN 0-7923-9641-3
- W.J. Dally, J.W. Poulton, Digital Systems Engineering (Cambridge), ISBN 0-521-59292-5

**Course notes, papers, project assignments, etc.:** The wolfware course locker will be used to distribute course notes, papers, and assignments. *Please make sure that you print the first set of notes before the first class from the website.* Also note that the notes distributed on-line are NOT the complete notes for the class. Classroom attendance and note-taking is expected.



You will find the course website and bulletin board on wolfware, as linked from the page [www.courses.ncsu.edu/ece733](http://www.courses.ncsu.edu/ece733) . I emailed the class last week. If you did NOT receive these emails, check your “official” email address at [www.ncsu.edu](http://www.ncsu.edu) “directories” in the top right corner.

**Prerequisite:** Grade of B or better in ECE 546 or equivalent. Functionally, I am assuming that students are familiar with the basics of MOSFET operation and MOSFET circuit design, e.g. linear and saturation modes, and the design and operation of CMOS static logic gates. I will assume that you also have access to, and know how to use, a suitable circuit simulator, such as Hspice, and know how to perform schematic capture and simulation within the NCSU Cadence environment.

**Course Objectives.** Provide an in depth study of selected topics in the design of digital CMOS circuits, at the transistor level. Topics will include CMOS scalability; high-speed logic design; memory design; and high-speed I/O design.

### Course Outcomes

- Student will understand the impact of technology scaling on circuit design
- Student will be able to describe the different types of high-speed circuit styles and how to design in them
- Student will be able to design a high-speed synchronous logic circuit to specifications
- Student will be able to describe how to design the different sub-circuits in memory blocks
- Students will be able to describe the factors that go into high-speed I/O design
- Students will be able to describe the different approaches to high-speed I/O design
- Students will be able to design a high-speed I/O system to specifications

**Course Projects:** In order to provide an in-depth experience, you will also carry out two small design projects. The projects are not finalized yet but are likely to be a high-speed CMOS flip-flop design, and a CMOS transceiver design. An informal lab will be organized to provide active help for the projects and provide a forum for evaluation of the projects. Though lab attendance is not required, little assistance will be available outside of the labs.

### Homework TurnIn

- On-campus students. Unless specifically requested, please bring a paper copy to class.
- EOL students: Please use online turn in if you can. Otherwise, mail or fax it to the EOL office. The turn-in date is the postmark date, not receipt date.

### Course Syllabus

1. Introduction
2. Static logic gates
3. Dynamic logic gates
4. Flip-flops
5. Timing and design
6. Interconnect
7. Transceiver Design

**Software Requirements.** You will need access at least to a Spice simulator for this course, and preferably also a schematic capture tool. On campus students will be encouraged to use Hspice, and Composer. Off campus students will be given access to these tools but can also use their companies or third party tools (e.g.

<http://www.duncanamps.com/spicesim.html> lists a number of free Spice tools).

**Student Evaluation.** You will be evaluated as follows:

- *Homeworks.* There will be a small number of homeworks to force review of specific issues. (20%)
- *Midterm.* (20%)
- *Projects.* You will be individually graded on two small projects. Each project is worth 20% of the grade. (40%).
- *Final exam.* On material covered since the midterm. (20%)

|              |                        |          |
|--------------|------------------------|----------|
| Midterm Exam | February 27            | In class |
| Final Exam   | Monday, April 27, 6 pm | In class |

Collaboration is encouraged on the homeworks and projects but you are expected to turn in individual solutions and reports. **Sharing of electronic files is expressly forbidden.** It is easy to tell if a circuit design has been copied. The exams will be open-book, open-notes, multiple-choice and short answer exams.

#### **Instructor Research Interests**

- Application specific processors. Current projects focus on applications and design of 3DICs.
- Interconnect, including transceivers, electronic packaging, on-chip interconnect, and between-chip interconnect.
- Nanocomputing – how to build the computers that will eventually displace or complement CMOS.

#### **Students with disabilities**

Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653. [http://www.ncsu.edu/provost/offices/affirm\\_action/dss/](http://www.ncsu.edu/provost/offices/affirm_action/dss/) For more information on NC State's policy on working with students with disabilities, please see [http://www.ncsu.edu/provost/hat/current/appendix/appen\\_k.html](http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html)

#### **Academic integrity**

All the provisions of the [code of academic integrity](#) apply to this course. In addition, it is my understanding and expectation that your submission on any test or assignment means that you neither gave nor received unauthorized aid. For homeworks and projects, while collaboration is encouraged, sharing of design data is expressly not permitted. In particular sharing of any electronic files, or schematics is forbidden.