

ECE 733

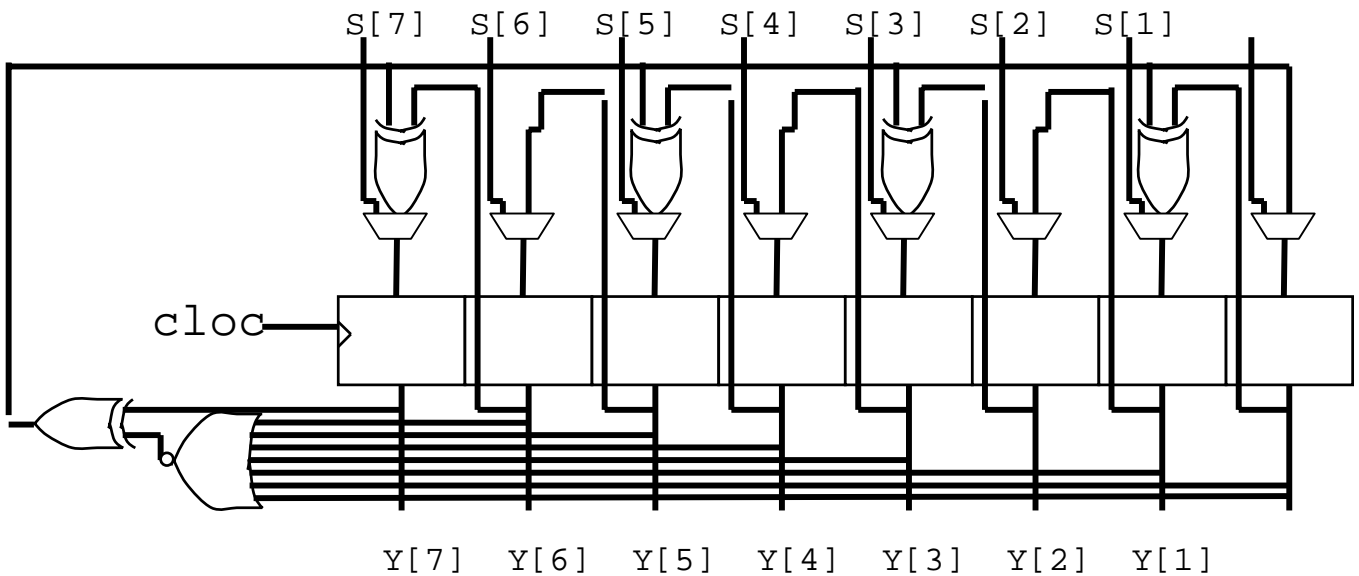
Project 1

Due : Tuesday, March 30, 2004, in class

LFSR Design

Design an 8-bit LFSR with the nominal TSMC 0.18 mm process parameters (tsmc18p and tsmc18n), and nominal temperature (25 C). The circuit is sketched below. You must be able to load a seed to it (S) and then let the circuit free-run with a clock. It is OK to load the seed via SR inputs to the FFs rather than a mux as drawn, though you will need to generate the two-bit inputs from S[I] yourself, via appropriate logic, and count that in your design power and speed. Please load the Y outputs with minimum sized inverters. Please drive your clock(s) through an inverter pair (you can size these yourself). Similarly, the gates do not have to be exactly as drawn, as long as the same logical intent is met. (e.g. Actually using one 7-input gate is obviously silly.) Due to the potential for race, you must use edge triggered flip-flops or a two phase non-overlapping clocked latch design.

The circuit is to perform at a speed of at least 4 GHz.



Deliverables

Report describing the approach used, including circuit topology, samples of simulation results, achieved speed and energy consumed for the first 100 cycles when loaded with a seed of 10101010. Include simulation results showing the circuit working at the claimed speed. Make sure that the drains and sources are correctly sized (e.g. by using schematic capture). Make sure that you include all your inverters in your energy simulation. Also make sure that you use the energy evaluation method posted on the class web-page.

Evaluation

You will be evaluated out of 100 and assigned a grade based on the following criteria:

90/100 : This is the grade that will be given to a basic, working complete project. I.e. If it meets the following standards:

- Correct operation at 4 GHz. You can assume zero clock skew.
- A clear report describing the circuit approach used, and results obtained.

80-89/100 : Missing one or two major attributes above. E.g. Being slower, or not conveying an understanding of how the circuit works and how you designed it, or submitting a scrappy report.

0-79/100 : A submission that clearly does not achieve the goals established here. E.g. Does not work, very slow maximum speed.

91-110/100 : You will compete for points beyond 90 on the basis of energy-delay product. I.e. The product of energy per cycle (total energy for 100 cycles / 100) and the clock period. It is OK if your circuit operates at a speed beyond 5 Ghz. You are to report this figure and the supporting calculation. If the worst 5GHz design has an energy delay product of X and the best an energy delay product of Y, and yours an energy delay product of Z, then your grade will be $90 + 20*(Z-X)/(Y-X)$. **It will be very useful if some of you report the energy-delay product of an unoptimized, but reasonable, 4 GHz design in your report. (If I feel generous, I will use one of those figures as 'X')**. Note the "91-110" is not a typo.

Collaboration

If you help each other that is fine, in fact encouraged. However, I expect that each of you do your own design capture, optimization, simulations and interpretation for the final report. In fact, I would expect each design to be unique in some small features, at least. If it is clear that someone rode completely on another students back, both students will be penalized. I request that you DO NOT share electronic versions of your designs or results. E.g. Explaining, in detail, how your design works to a friend is good, emailing that friend your schematic file is very bad.