

## ECE 733 Project 2

**Due : Thursday, April 29, 2004, in class**  
(Up to one week late with a 10% penalty)

### Transceiver Design

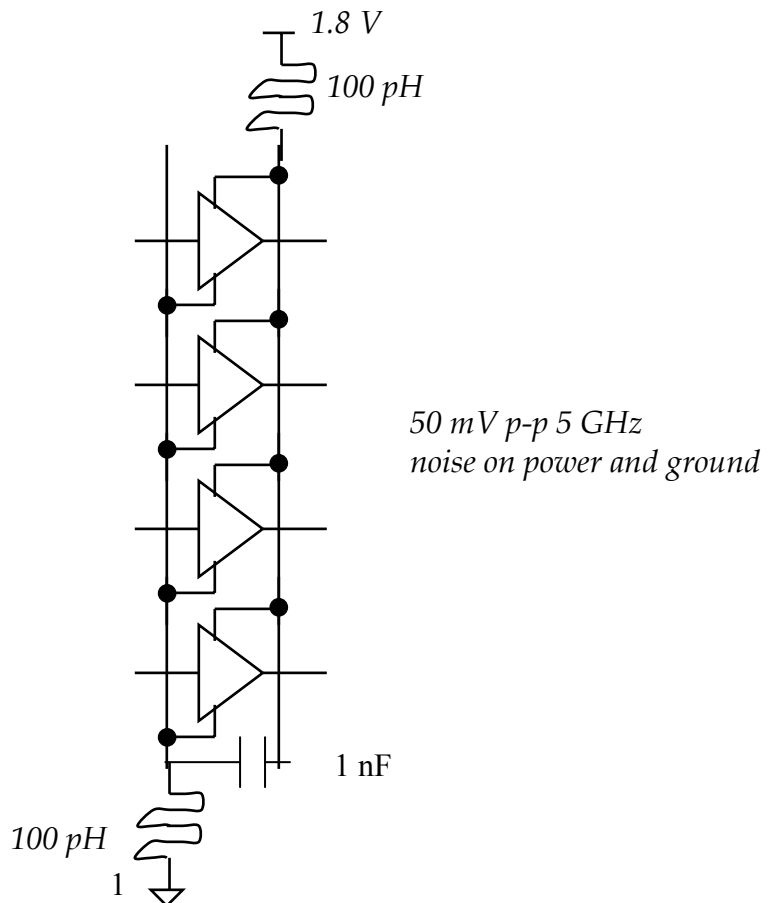
Design a 4-bit wide 0.18  $\mu\text{m}$  transceiver that operates at the fastest possible bit rate, while meeting the following constraints:

- Over 50 cm lossy transmission line.
- Operating at an actual data rate of at least 3 Gbps.
- Use the tsmc18n and tsmc18p circuit models.
- Subject to a 50 mV peak-to-peak 5 GHz sinusoid ripple on the power and ground at both TX and RX. The 5GHz sinusoidal 50 mV noise sources on the supply rails must be 180 degrees out of phase. (Shows headroom compression and expansion)
- You can ignore ESD protection.
- While sharing a 100 pH inductance to the power and ground at both TX and RX.

Note the 1 nF on-chip decoupling capacitor.

- While meeting an eye specification of an eye aperture opening specified below (as measured at the final output of your RX) while executing an identical pseudo-random bit sequence on all 4 inputs simultaneously. The pseudorandom sequence should be at least 500 bits long. However, when investigating the design tradeoffs, you might want to use a shorter sequence. You can use the “.include” feature in Hspice to read in a data file generated elsewhere.

- Correct transistor perimeter and area parameters must be included in the spice netlist.
- Ideal voltage and current sources cannot be used to supply biases to internal circuitry. These lead to inaccurate power consumption measurements.
- Interconnect parasitic capacitors should be terminated to the on-chip ground on one side and to the transmission line ground on the other.
- Supply rails (power and ground) for all transceiver circuitry must be taken from the supply pin (modeled as a 100 pH inductor).

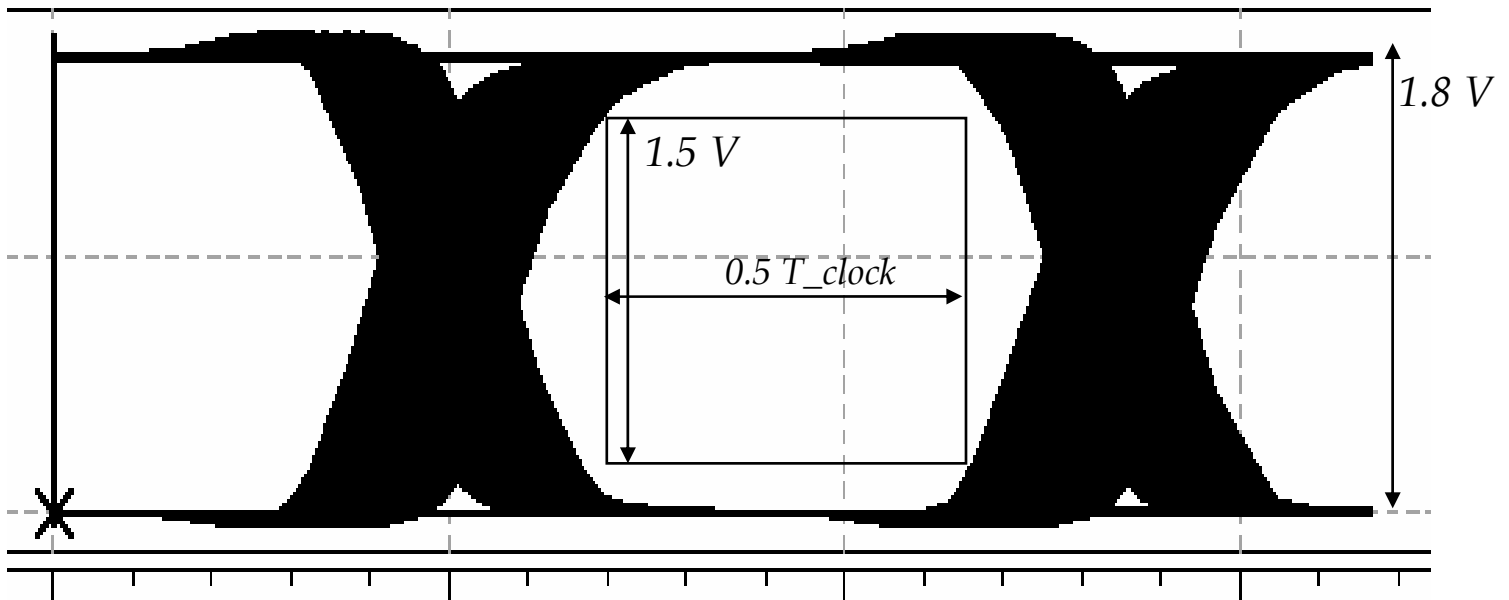




devices (pmos, nmos) automatically connect the bulk to the **ideal rails** (Vdd, gnd), which is inaccurate.

A similar LC structure can be connected in parallel to the above circuit (at the OFFchippower and OFFchipgnd nodes) to provide the supply rails for the receiver. The supply nets Vccd and gnda could be used in a similar manner across the receiver on-chip decoupling capacitor. Again, with exception of the gnd supply net, the supply nets are equivalent to labeling nodes. They merely offer a bit of convenience.

### Required Eye Opening at final RX output



### Producing an Eye Diagram

The following code fragment will allow you to produce an eye diagram:

```
V1 EYE_X_AXIS 0 PULSE 0 'period*2' 'period*offset+fine_offset'  
'period*2-step' step 0.0n 'period*2'
```

ADD ABOVE LINE INTO YOUR SP FILE;  
USE EYE\_X\_AXIS AS X\_AXIS, AND THE SIGNAL AS Y\_AXIS, THEN YOU WILL  
SEE THE EYE.

\* where period is the width of a bit; offset is from which bit you want to see EYE, say 1,2,3,... or whatever you want; fine\_offset is used to set the sampling point; step is used to set the resolution

\*Example: To see the EYE of a 5Gbps NRZ signal

\*Set the parameters to

\*period=200ps

\*offset=0

\*fineoffset=0ps

\*step=1p

\*You need to set your own offset, fine\_offset and step to get best EYE and reduced run time.

### **Deliverables**

A report describing the approach used, including circuit topology, simulation results, achieved speed and total power consumption. Also describe the power consumed **at 3 Gbps**, using the same methodology as used in the first project.

- Reports should begin with a “Contents” page listing headings with corresponding page numbers and number **all** pages (by hand if necessary).
- All results should be presented in the **body** of the report (in tables if possible). Relevant schematics, plots, netlists, text files, etc. should be clearly referenced and included in the appendix. Binary text files do not need to be included.

### **Evaluation**

You will be evaluated out of 100 and assigned a grade based on the following criteria:

**90/100** : This is the grade that will be given to a basic, working complete project. I.e. If it meets the following standards:

- Meets the above specifications while operating at 3 Gbps (actual symbol rate).
- A clear report describing the circuit approach used, and results obtained. The report should include the power report. The report should be neat and written on a computer – no hand-drawn diagrams.

**80-89/100** : Missing one or two major attributes above. E.g. Being slower, consuming more power, or not conveying an understanding of how the circuit works, or submitting a scrappy report.

**0-79/100** : A submission that clearly does not achieve the goals established here. E.g. Does not work, very slow maximum speed.

**91-110/100** : Some clearly superior feature. Examples include the following:

- Some of these points will be allocated for exceeding the speed goal above, probably on a competitive, most likely linear, basis. e.g. The design that achieves the fastest circuit [of say Y Gbps] **might** get 20 more points, while a design that achieves a slower speed of Z Gbps might get  $20 \cdot (Z-500)/(Y-500)$  more points. I’ll decide how many points to allocate to speed after seeing the reports. A similar weighted scale will be used for power consumption. However, speed will have twice the weight of power consumption.
- New circuit topologies. For example, a circuit that has a clear performance (or power) advantage over all existing published circuits, and I believe to be

publishable. (If that happens, I would actually want to submit it to Electronics Letters – we'll have the reviewers' comments back in 6 weeks.) We might actually build a very high quality circuit.

- Some other clearly superior attribute. E.g. A better and unique optimization strategy.

### **Collaboration**

If you help each other that is fine, in fact encouraged. However, I expect that each of you do your own design capture, optimization, simulations and interpretation for the final report. In fact, I would expect each design to be unique in some small feature. If it is clear that someone rode completely on another students back, both students will be penalized. I request that you DO NOT share electronic versions of your designs or results. E.g. Explaining, in detail, how your design works to a friend is good, emailing that friend your schematic file is very bad.

### **Different Eye Opening Criteria**

You can use a different eye opening criteria if you can justify it. However, you have to justify it in terms of aperture time, jitter, sensitivity, etc. of an actual circuit. Be careful as I have not given you the process corners (one way to cope with this is assume they have an effect equal to a temperature spread, e.g. the pFET and nFET at different ends of the commercial temperature range). Since you are not building the clock recovery circuit, you can only estimate the effective jitter. Perhaps assume, it is equal to the aperture time of your FF. A full and proper treatment arising at a different eye criteria will be considered worthy of bonus points.

### **Single Sided Interconnect Circuit Model**

#### Interconnect Circuit

For a single sided transmission line, use the following W-model:

```
W1 N=1 TL_IN 0 TL_OUT 0 RLGCMODEL=ECE733 l=0.5
```

```
.MODEL ECE733 W MODELTYPE=RLGC N=1  
+Lo=  
+300e-9  
+Co=  
+120e-12  
+Ro=  
+0.54  
+Rs=  
+0.000462  
+Gd=  
+1.4e-11
```

This is the W model (for microstrip line on PCB),  
TL Length is 10cm, Z0=50ohm, propagation speed is 1.67E+8m/s.

The corresponding PCB trace is:

1. thickness of the top metal layer(copper): T is 2~2.5mil,
2. width of the top metal layer: W=22mil,
3. thickness of dielectric layer: H=12mil,

This model is based on Freq=4GHZ. Gd is frequency dependent loss.

**W Model for differential TL:**

```
W1 N=2 TL_IN_POS TL_IN_NEG 0 TL_OUT_POS TL_OUT_NEG 0
RLGCMODEL=ECE733 l=0.5
```

```
.MODEL ECE733 W MODELTYPE=RLGC N=2
+Lo=
+300e-9
+60e-9 300e-9
+Co=
+120e-12
+ -24e-12 120e-12
+Ro=
+0.54
+0 0.54
+Rs=
+0.000462
+0 0.000462
+Gd=
+1.4e-11
+ -0.14e-11 1.4e-11
```

Explanation:

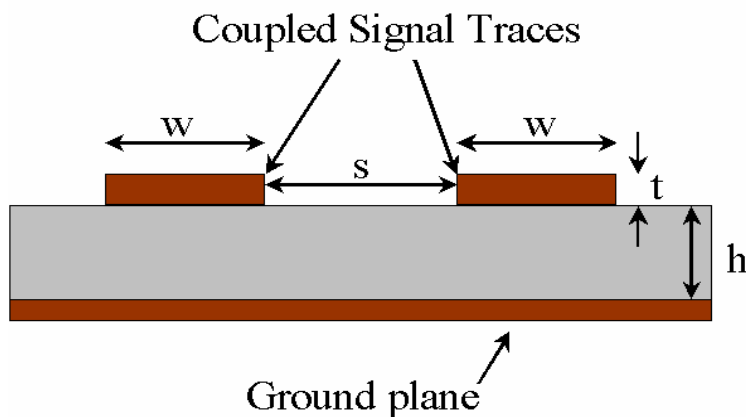


Fig.1 Actual Size

w=22mil, h=12mil, t=2~2.5mil, s=5\*w,  $\epsilon_r=4.6$

1. Assume Coupled dielectric loss is 10% of the self dielectric loss, that is mutual  $G_d=1.4e-11*10\%=0.14e-11$ . This mutual  $G_d$  is enough, given the space of the coupled traces is not place very near:  $w=5*s$ .
2. Mutual capacitance and mutual inductance of the coupled differential TL is derived from the actual geometrical, see detail derivation in the matlab file. The result is shown in Fig2 and Fig3. Fig2 shows Odd mode impedance and Even mode impedance Vs.  $S/W$ . We don't need to consider Even mode impedance too much since the common mode voltage on TL is zero for ACCI. Fig.3 shows the coupling coefficient: for lines in homogeneous medium,  $K_m=K_c$ . For case of  $S=5*W$ ,  $K_m=K_c=0.2$ ,  $Z_{odd}=41\text{ohm}$ (that is Differential impedance is 80ohm).

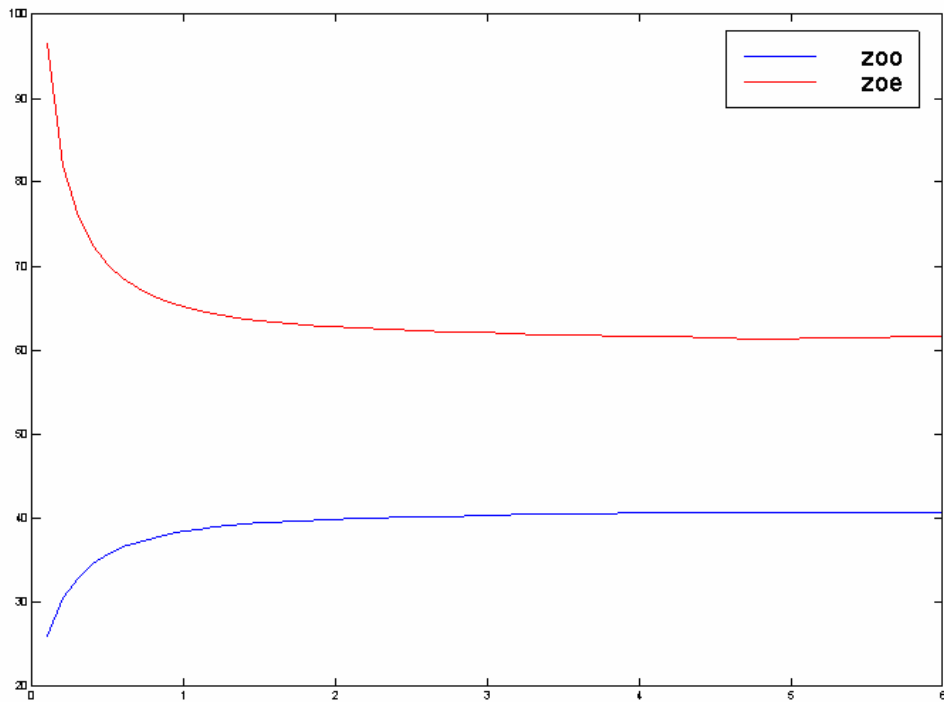


Fig2. Zodd and Zeven VS. S/W

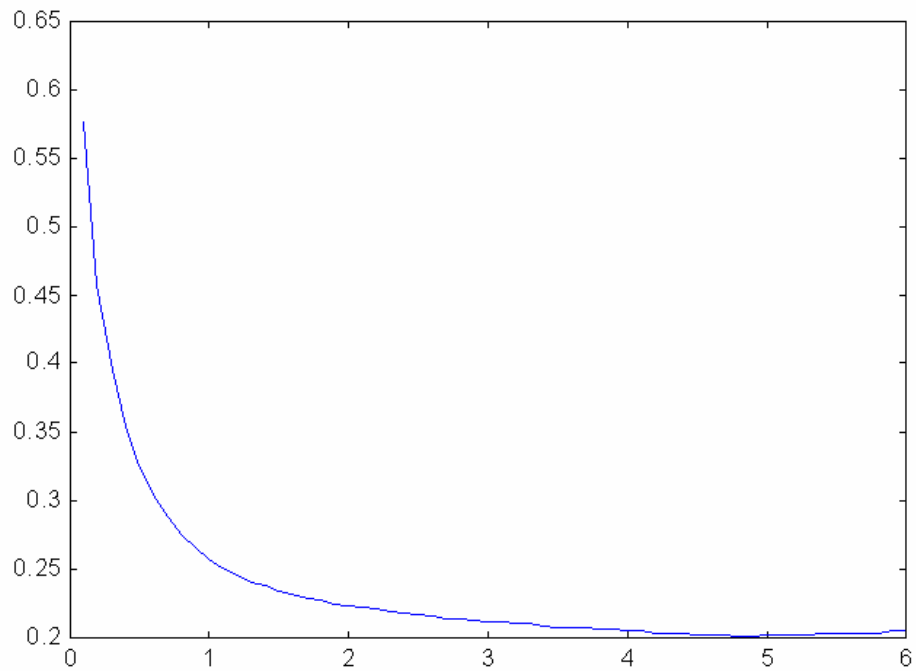


Fig.3 Kc and Km VS. S/W

Smaller S will lead to larger Kc,Km and smaller differential impedance.

3. This model is simulated in Hspice and when terminated by 41ohm, the reflection is the smallest, which proves the correctness. See attached spice file for details.

```

****Matlab file*****
clear all;
close all;
w=22;

h=12;
e0=8.854e-12;
er=4.6;
eeff=(er+1)/2 + ((er-1)/2)/sqrt(1+12*h/w);
z0=50;
c0=120e-12;
c=3e8;

cp=e0*er*w/h;
cf=0.5*(sqrt(eeff)/(c*z0)-cp);

for i=1:300
    s(i)=0.1*i*w;

```

```

k(i)=(s(i)/h)/(s(i)/h+2*w/h);
k1(i)=sqrt(1-power(k(i),2));
if power(k(i),2)<0.5
    kk(i)=(1/pi)*log(2*(1+sqrt(k1(i)))/(1-sqrt(k1(i))));
else
    kk(i)=pi/log(2*(1+sqrt(k(i)))/(1-sqrt(k1(i))));
end

cga(i)=e0*kk(i);
cgd(i)=(e0*er/pi)*log(coth((pi*s(i))/(4*h)) +
0.65*cf*(0.02*sqrt(er)*h/s(i)+1-power(er,-2)));

cm(i)=cga(i)+cgd(i);

kc(i)=cm(i)/c0;
km(i)=kc(i);

zoo(i)=z0*sqrt((1-km(i))/(1+kc(i)));
zoe(i)=z0*sqrt((1+km(i))/(1-kc(i)));

end

figure(1);
grid on;
plot(s/w, zoo, 'b');
hold on;
plot(s/w, zoe, 'r');
xlabel('s/w');
ylabel('zo');
legend('zoo', 'zoe');

figure(2);
grid on;
plot(s/w, kc, 'b');
xlabel('s/w');
ylabel('kc and km');

****Spice file****

.param Rterm=35

R10 V_NEG IN_NEG Rterm M=1.0
R0 V IN Rterm M=1.0

V2 V_NEG 0 PULSE 1.0 0.0 0.0 50E-12 50E-12 50E-12 10E-9
V0 V 0 PULSE 0.0 1.0 0.0 50E-12 50E-12 50E-12 10E-9

```

```
R7 OUT_NEG 0 9E6 M=1.0
R5 OUT 0 9E6 M=1.0
```

```
W1 N=2 IN IN_NEG 0 OUT OUT_NEG 0 RLGCMODEL=ECE733 l=0.1
```

```
.MODEL ECE733 W MODELTYPE=RLGC N=2
```

```
+Lo=
+300e-9
+60e-9 300e-9
+Co=
+120e-12
+ -24e-12 120e-12
+Ro=
+0.54
+0 0.54
+Rs=
+0.000462
+0 0.000462
+Gd=
+1.4e-11
+ -0.14e-11 1.4e-11
```

```
* INCLUDE FILES
```

```
* END OF NETLIST
```

```
.TRAN 1.00000E-12 1.00000E-08 START= 0.
.TEMP 25.0000
.OP
.save
.OPTION INGOLD=2 ARTIST=2 PSF=2 post
+ PROBE=0
```

```
.alter
.param Rterm=37
.alter
.param Rterm=39
.alter
.param Rterm=41
.alter
.param Rterm=43
```

```
.END
```

Note: the equations in Matlab file is originally used to calculate large coupling lines, so when  $S > 6*W$ , the result is not quite correct. However, it gives the correct result for  $S < 6*W$ .