

Interconnect Circuit Design

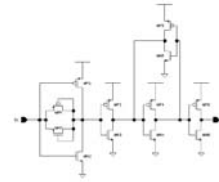
Dr. Paul D. Franzon

Outline

- Wires & Noise
- Signaling alternatives
- Driver & Receiver circuits

References

- Dally & Poulton, Chapters 3, 5, 6, 7, 8



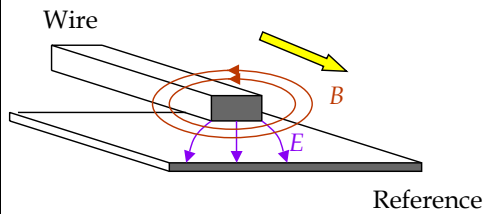
Outline

Wires and Noise

- Interconnect equivalent models
 - ◆ Signal Propagation
 - ◆ RLC, Z0
 - ◆ Differential lines
- Discontinuities
- Noise Sources :
 - ◆ Common Mode noise
 - ◆ Reflections
 - ◆ Crosstalk

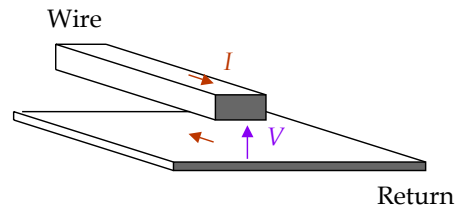
Signal Propagation

Two equivalent views of signal propagation:



Propagating EM Field

- E field to reference
- B field
- Propagating at speed of light
- Attenuated by losses
 - Conductive loss in wires & return
 - Dielectric loss



Propagating IV Wave

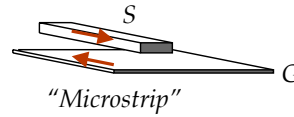
- Voltage, $V = \int E \, dx$
 - Current, $I = \mu \int B \cdot dl$
- Circuit View:
- $R \propto$ Conductor Losses
 - $G \propto$ Dielectric Losses
 - L, C per unit length
 - \propto energy stored in E and B fields

Return Path

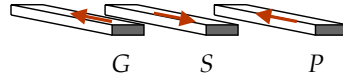
KCL → Current on signal line must return to driver

Return paths :

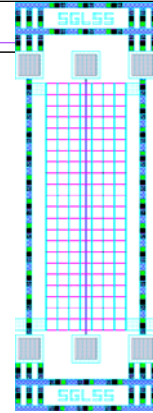
- Reference or “ground” (or “power”) plane
 - Is often a grid on chips



- Coplanar lines

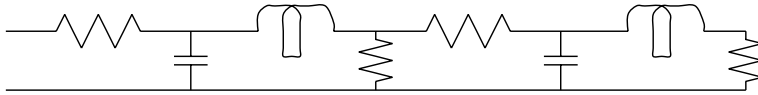


- E.g. between Power/Ground grid on-chip
- Neighboring lines
 - Will appear as Crosstalk then



Equivalent Circuit

Distributed RLGC



Equivalent Transmission Line Equations :

Solving for:

$$\frac{dV}{dx} = -ZI \quad \frac{dI}{dx} = -YV$$

Gives : $V = V_+ e^{-\gamma x} + V_- e^{\gamma x}$

$$I = \frac{1}{Z_0} (V_+ e^{-\gamma x} - V_- e^{\gamma x})$$

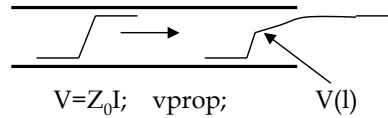
Propagation Constant $\gamma = \sqrt{ZY} = \sqrt{(R + j\omega L)(G + j\omega C)}$

Impedance $Z_0 = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$

Low Loss Approximation

If :

$$G \ll j\omega C \quad \text{and} \quad R \ll j\omega L$$



Then

$$Z_0 = \sqrt{\frac{L}{C}} \quad \gamma = \alpha + j\beta$$

Where

$$\alpha = \frac{R}{2Z_0} + \frac{GZ_0}{2} \quad v_{prop} = \omega / \beta = 1 / \sqrt{LC} = c / \epsilon$$

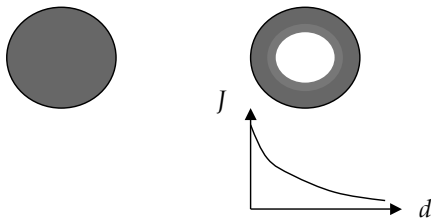
Wave travelling down transmission line at speed of light in medium v_{prop} and losses at position l ,

$$V(l) = V(0)e^{-\alpha l}$$

Resistance

Components of Line Resistance

- DC Resistance of Signal Wire $R_{DC} = \frac{\rho}{wt}$
 - Al : $\rho = 4.3\text{E-}8 \text{ } \Omega\cdot\text{m}$
 - Cu : $\rho = 1.7\text{E-}8 \text{ } \Omega\cdot\text{m}$
- Return Path Resistance
 - Can only be solved numerically
- Skin Effect
 - Current distribution tries to minimize Energy lost or stored to transmit signal
R+jwL component → Current crowding at higher frequencies



Skin depth, δ

$$J = e^{-d/\delta}$$

$$\delta = \sqrt{\pi \frac{f\mu}{\rho}}$$

Skin Resistance

Skin Depth does not matter until skin depth $\sim t/2$, where t is conductor thickness

- Occurs at frequency f_s

$$f_s = \frac{\rho}{\pi\mu(t/2)^2}$$

E.g. 2 μm thick (IC) Copper $f_s = 1.7\text{E-}8 / \pi 4\pi\text{E-}7 (1\text{E-}6)^2 = 4.3 \text{ GHz}$

E.g. 30 μm thick (PCB) Copper $f_s = 4.7 \text{ MHz}$

Above this frequency,

$$R_s \approx R_{DC} \sqrt{\frac{f}{f_s}}$$

Attenuation,
$$\alpha_s = \frac{R_{DC}}{2Z_0} \sqrt{\frac{f}{f_s}}$$

Dielectric Loss

Expressed as Loss Tangent:

$$\tan \delta_D = \frac{G}{\omega C}$$

Attenuation :

$$\alpha_D = \frac{\pi f \sqrt{\epsilon_R} \tan \delta_D}{c}$$

ϵ_R =relative dielectric constant, c = speed of light in vacuum

E.g. FR4 $\epsilon_R=4.7$, $\tan \delta = 0.035$

Using above equations, dielectric loss exceeds skin loss in a $100 \times 30 \mu\text{m}$ thick FR4 PCB line ($Z_0=50 \Omega$), at a frequency of 6.8 GHz.

Practical Wire Models

Need to decide on most useful model for each piece of interconnect:

Issues involved :

- Loss mechanisms and values
- Frequency range over which model has to be useful
 - Remember for a signal $f_{3dB} \approx 0.35 / t_r$
 - Then signal wavelength $\lambda = v_{prop}/f$
 - E.g. 100 ps signal in FR4, $\lambda @ 3dB \text{ point} \approx 4 \text{ cm}$
- Length of line
- Line Uniformity w.r.t wavelength
 - Treat as distributed circuit (e.g. transmission line) if length $> \lambda/10$
 - Otherwise can treat as a lumped circuit

Printed Circuit Boards

- Low losses
- Typical Rise Time 100 ps
 - $\rightarrow \lambda_{3DB} \approx 4 \text{ cm}$

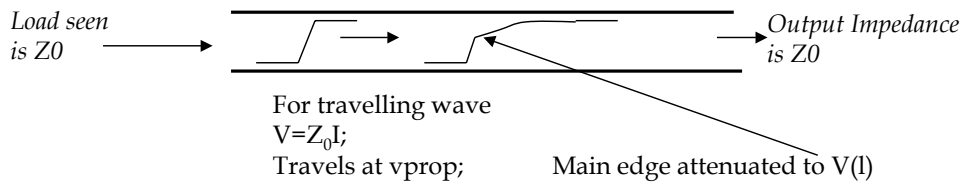
Typically, $Z_0 \sim 40 - 60 \ \Omega$

Treat as a low-Loss Transmission Line

- For best accuracy, will have to treat losses as being frequency-dependant as $f_{3DB} \gg f_{skin}$

Most Suitable Model :

- ◆ Transmission Line with Losses

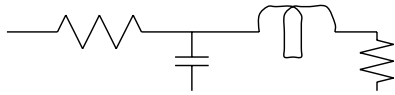


Vias, Connectors and Packages

Length typically less than $\lambda/10$

→ Usually best treated as lumped equivalent circuit

Might need a few “lumps” at faster edges or larger structures



- Note :
 - ◆ Generally vias, dominated by excess capacitance
 - (“Excess” over $L/\sqrt{Z_0}$)
 - ◆ Generally packages, wire-bonds, have “excess” inductance
 - ◆ Connectors can have either (but usually “excess” capacitance)

Sample Frequency Response of 30" Backplane Trace

Skin Effect

(3 dB/octave)

Dielectric Loss

(6 dB/octave)

Connectors, vias, etc.

$S_{21} = P_{out}/P_{in}$
For trace

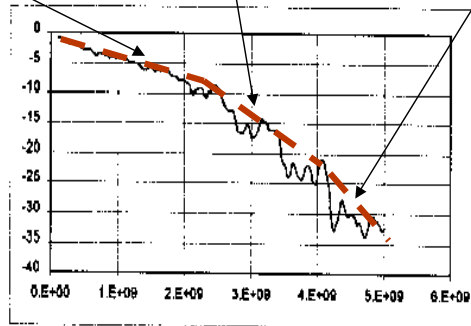
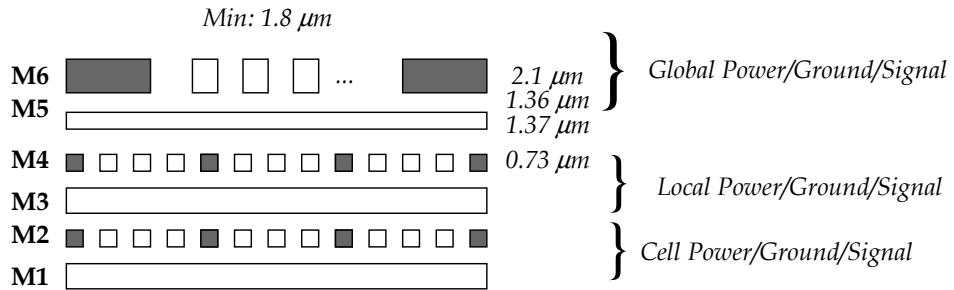


Figure 3 – Typical S_{21} , transmission plot for serial link
picture of what is happening in the frequency domain.

Typical IC Conductor Stack-Up

Sample 6-layer process:

Note : Even one thick metal can be “hard to get”



Short Runs on ICs

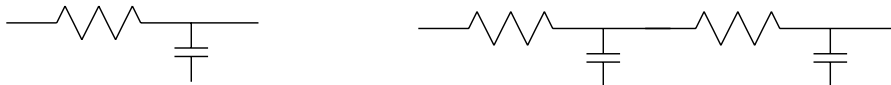
e.g. $1\ \mu\text{m} \times 1\ \mu\text{m} \times 100\ \mu\text{m}$ long wire

High & constant Losses

- $R_{\text{DC}} \sim 43,000\ \Omega / \text{m}$
- Say $L \sim 5\ \text{nH} / \text{m}$
 - ♦ $\rightarrow R > j\omega L$ until over 200 GHz
- 10 ps rise time $\rightarrow \lambda_{3\text{DB}} = 4\ \text{mm}$: Length $\ll \lambda/10$
- But, note 1 ps rise time $\rightarrow \lambda/10 = 40\ \mu\text{m}$!

Model = One or few lump RC circuit

- C Determined by proximity to neighboring wires (typically 2-5 pF/m)



RC propagation (speed of light signal attenuated by high losses)

Long Runs on ICs

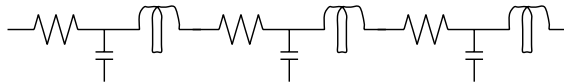
e.g. $10\ \mu\text{m} \times 2\ \mu\text{m} \times 1000\ \mu\text{m}$ long wire

High & constant Losses

- $R_{\text{DC}} \sim 2,000\ \Omega / \text{m}$
- Say $L \sim 5\ \text{nH} / \text{m}$
 - ♦ $\rightarrow R > j\omega L$ until over 1 GHz
 - ♦ So L does matter
- 10 ps rise time; $f_{3\text{DB}} = 35\ \text{GHz}$. $\rightarrow \lambda_{3\text{DB}} = 4\ \text{mm}$: Length $> \lambda/10$

Model = Several lump RLC circuit

- C Determined by proximity to neighboring wires

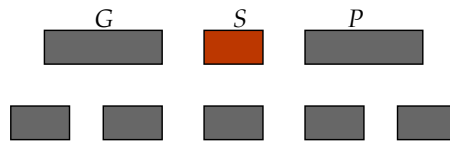


Long Wires on ICs

Best to turn into a uniform transmission line

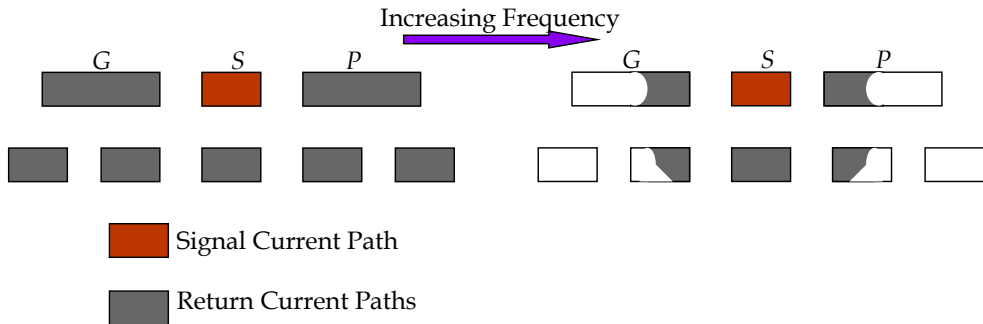
→ Defining Return Path

E.g.



Proximity Effect

More important than skin effect in determining frequency dependence



Return path resistance function of frequency

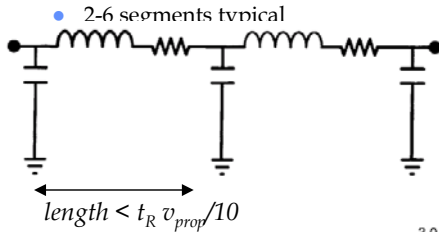
(However, single frequency modeling usually satisfactory - choose frequency between $1/(2t_r)$ and $1/(3t_r)$)

Note: Can **not** make signal wire arbitrarily wide to obtain low-R.

Example

Transmission Line Propagation

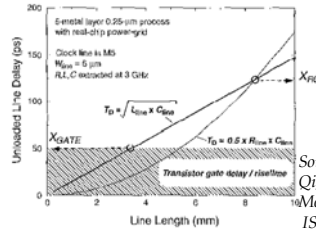
- \sqrt{LC} delay
- Model



- Potential for Reflection Noise
(Requires large driver,
 $Z_{drive} \sim \sqrt{L/C}$)

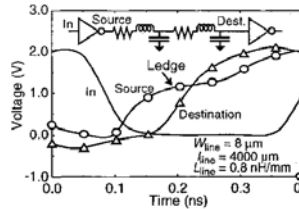
RC Propagation

- RC Delay



Source: Qi, et al. "On-Chip Inductance Modeling of VLSI Chips," ISSCC 2000

Figure 10.4.1: Line delay for different delay models.



Source: Cleveland, et al. "Line Inductance Modeling And Extraction in a Real Chip with Power/Ground Grid", IEDM 98.

Fig. 9. Simulations of RLC delay line.

Example ... Clock Nets

Including L is important to accurately predicting clock skew and both L and R_{return} are important for predicting transition time.

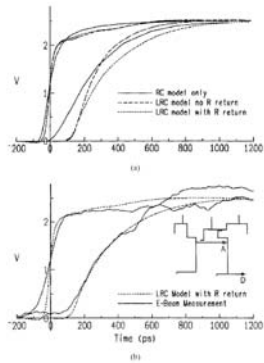


Fig. 5. Test chip waveforms along another branch of the tree, with (a) simulated RC model, LRC model without return path resistance effect, and LRC model with return path resistance effects. (b) Measured waveforms compared to the full LRC simulation. The inset shows the first-level clock tree and the measurement points. The oscillations seen in the measured waves are measurement artifacts.

Thin M4

Source: P. Restle, "Measurement and Modeling of On-Chip Transmission Line Effects in a 400 MHz Microprocessor," IEEE JSSC, 33(4), April 1998.

Thick M5

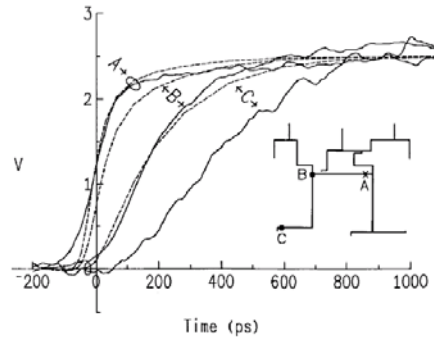


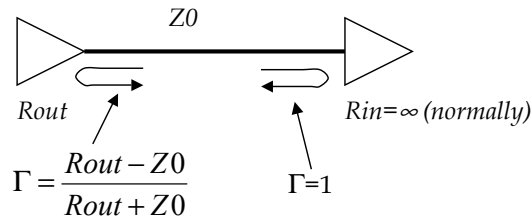
Fig. 4. Test chip waveforms (solid) with RC wire model (dashed) showing large delay error due to transmission line effects. Inset shows the first-level clock tree and the measurement points.

Measured using Ebeam. RL essential for clock delay estimation. 200 ps error on RHS!!! Strong "TL effects" L important to get delay correct on LHS and RL important to get transition time accurate, even though these are "thin" conductors and RC behavior expected.

Noise Sources

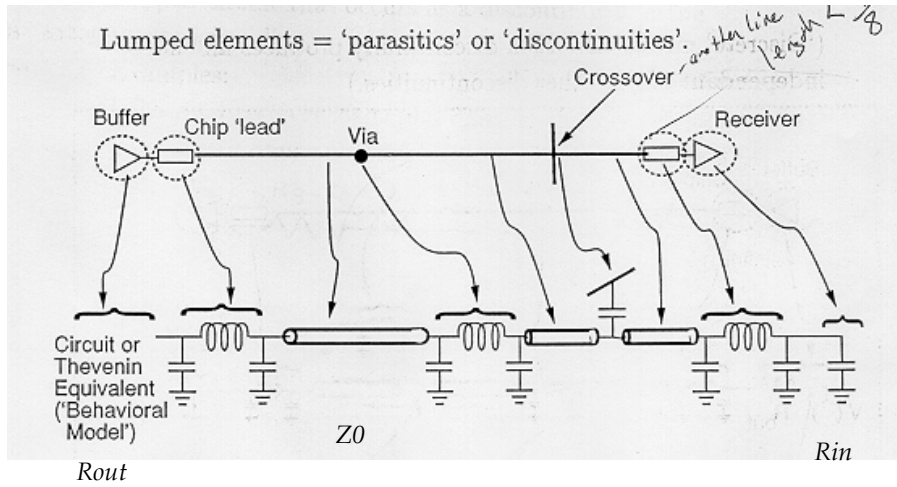
Reflection Noise

- Can occur in transmission line environments, at discontinuities and line ends : % of voltage wave reflected = Γ



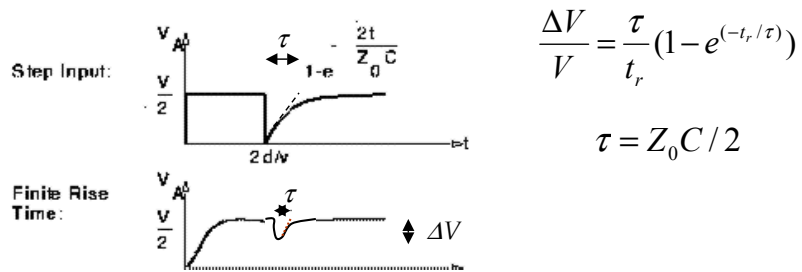
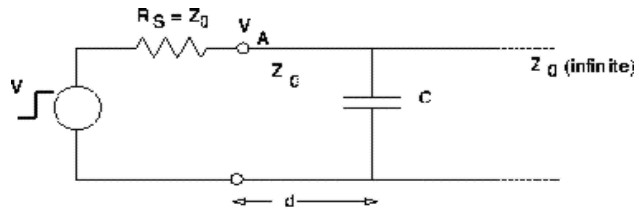
- In a high speed signalling, reflections need to be eliminated by making R_{out} or $R_{in} = Z_0$ (externally or internally to the chip)
- E.g. Make $R_{in} = Z_0$, and make R_{out} s.t. $V_{swing}(Z_0 / (R_{out} + Z_0)) > V_{IH}$
 - \rightarrow First Incident Switching (First wave arriving at the end of the transmission line can switch the receiver.)

Reflection Noise from Parasitics



Reflections at lumped loads

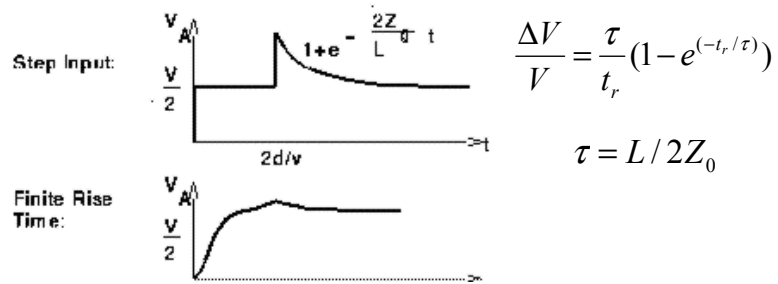
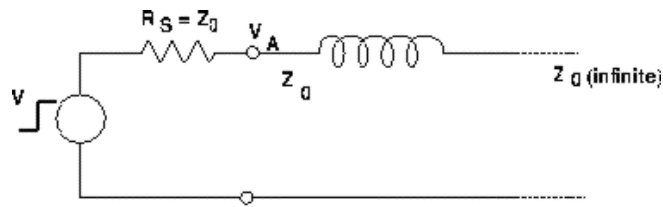
1. Reflections from lumped loads



$$\frac{\Delta V}{V} = \frac{\tau}{t_r} (1 - e^{-(t_r/\tau)})$$

$$\tau = Z_0 C / 2$$

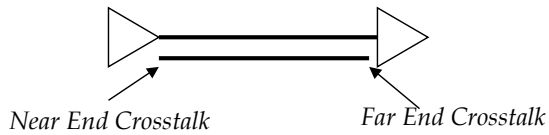
...Reflections from



Noise Sources

Crosstalk Noise

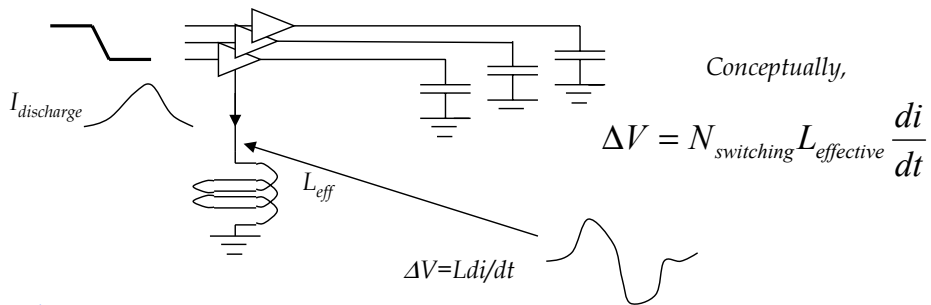
- Occurs in both lumped and distributed (transmission line) circuits



- In Transmission lines, normally $NEXT > FEXT$
- In lumped circuits, $NEXT = FEXT$

Simultaneous Switching Noise

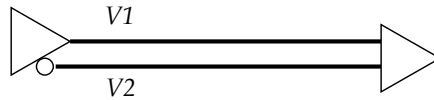
Loads discharging into packaging inductance:



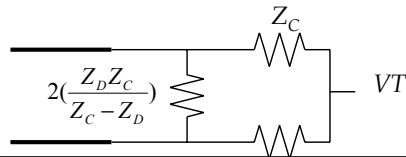
- Also Vcc noise
- Leads to common mode noise on power ground
- Can also be introduced by large transients on clock circuit

Differential Transmission Lines

Differential circuits Used to reject common mode noise



- Mutual M , C_m
- Common Mode Signal $V_c = (V_1 + V_2)/2$
- Differential Mode Signal $V_D = (V_1 - V_2)/2$
- DM Mode signal sees Impedance $Z_D = \sqrt{(L - M)/C + C_m}$
- CM Signal sees Impedance $Z_C = \sqrt{(L + M)/C - C_m}$
- (Typically $Z_D \sim 100 \Omega$)
- Prefer to terminate both modes



Summary ... via Problems

For a “half ounce” Cu PCB trace (15 μm thick) and 100 μm wide, what is f_s ?

What is the attenuation on this line, due to skin effect, at 1 GHz?

Summary

For a 50 Ohm line, at what frequency would dielectric loss exceed skin effect loss?

If $L = 5 \text{ nH/m}$, $RDC = 200 \text{ W/m}$, $C = 3 \text{ pF/m}$, at what rise time would you include L? For this rise time, at what length would you use a distributed model?

Summary

For a $50\ \Omega$ line terminated at the RX, what TX Rout would be needed to reach 0.8 V in First Incident Signal, with $V_{\text{swing}}=1\ \text{V}$?

If the termination was not there, this would give _____ noise?

What other noise sources are important?