Outline

Signalling

- Goals
- Noise Evaluation
  - Eye Diagrams
- Basic Approaches
- Coding

References

- Ch. 7,8 D&P

Goals

Transmit data at required bit rate

- At a low Bit Error Rate (BER)
  - BER = 10^{-15} or better
  - BER limited by
    - Clock jitter (phase noise)
    - Aperture for signal capture
    - Noise Margin (voltage noise)
- At low power consumption

Problems and Issues

- Commmon mode noise on power & ground
- Reflection and Crosstalk Noise
- Clock strategies
- Channel and channel compensation

Bit Error Rate

Best determined through experimentation

- Apply psedo-random test pattern
- Measure logical output for bit value errors
- Requires full 2^{N-1} patterns to be effective
  - One worst case pattern is possible

Can be evaluated via eye diagram

Eye Diagram Analysis

Procedure:

- Captures InterSymbol Interference (ISI)
  - "leftover" noise from previous bits
- Plot random sample of waveforms on top of each other
  - Make sure eyes are 'well open' (>40%)
- Ensure clock 'envelope' well within data 'envelope'
- Deskew receiver can open eye

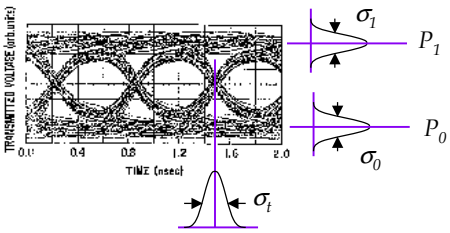
RMS Jitter = σ_t

- Jitter in both signal and clock in practice!
- (signal jitter included in -max values)

Bit Error Rate (BER)

- Related to Q Factor
- Q factor = $((P_1-P_0)/(\sigma_1-\sigma_0))$
- For evaluation only – not true BER!

Sample:



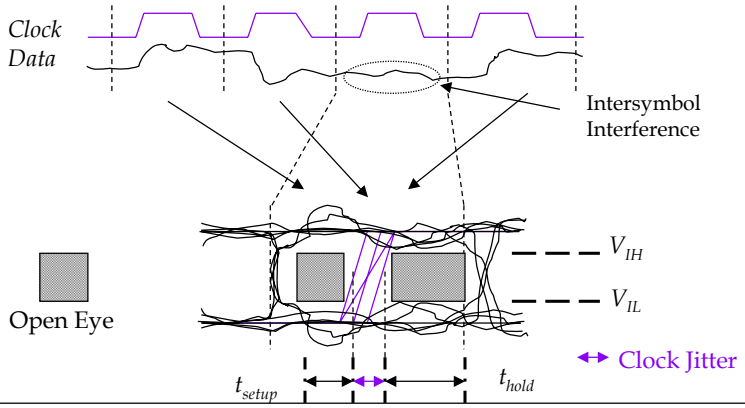
$$BER = \frac{1}{2} erfc\left(\frac{Q}{\sqrt{2}}\right) \approx \frac{\exp(-Q^2/2)}{Q\sqrt{2\pi}}$$

Q	BER
6	-10^{-9}
7	-10^{-12}

Constructing an Eye Diagram

Simulate data and clock for different process variations, different temperatures, different data patterns, etc.

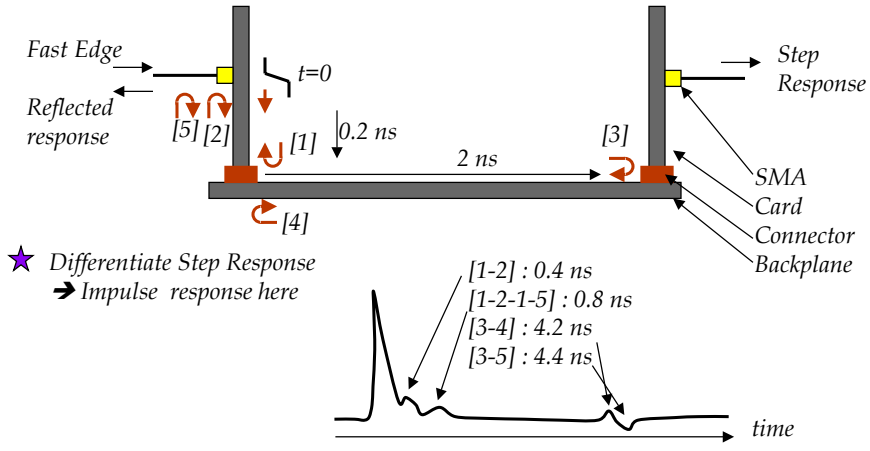
- Full path simulation, including package, connectors, vias, etc.
- Make sure to include clock skew and jitter



Eye Diagram

Can obtain from Channel Impulse Response:
Measurement technique (TDR & TDT):

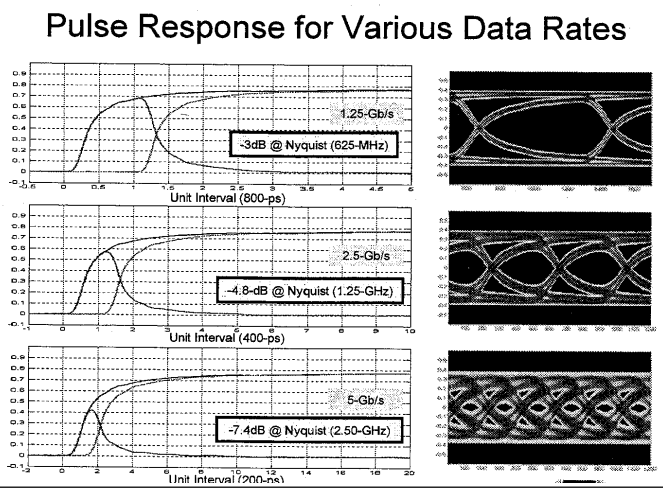
[1], [2], etc. : Reflection Events



Eye Diagram

Construct from Step Response

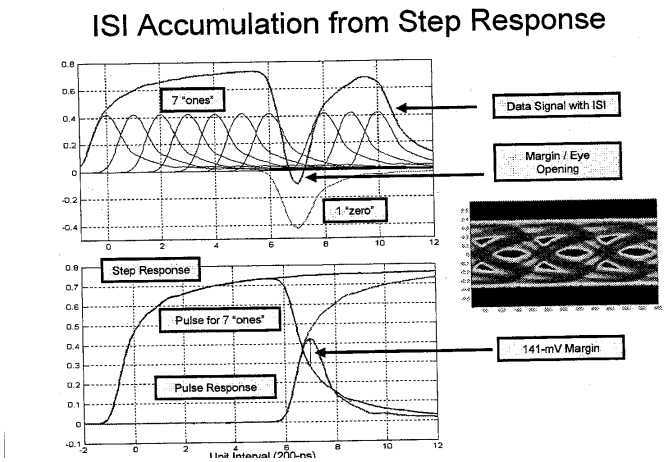
Pulse response = +step followed by - step



Eyes for 101010

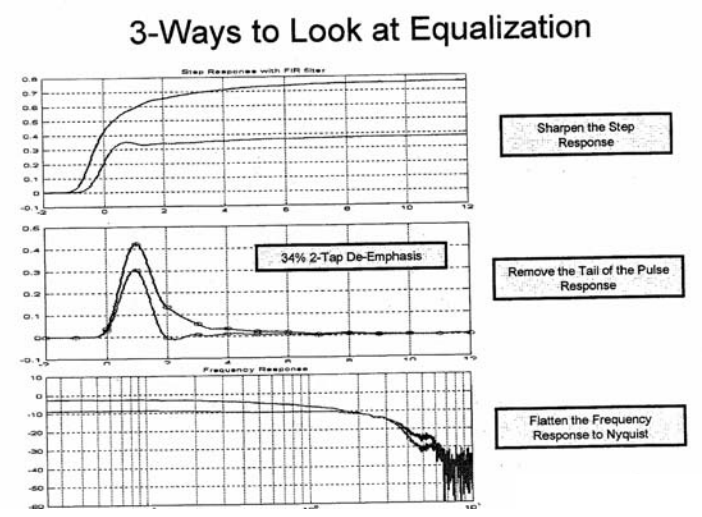
Eye Diagram

ISI Accumulation:

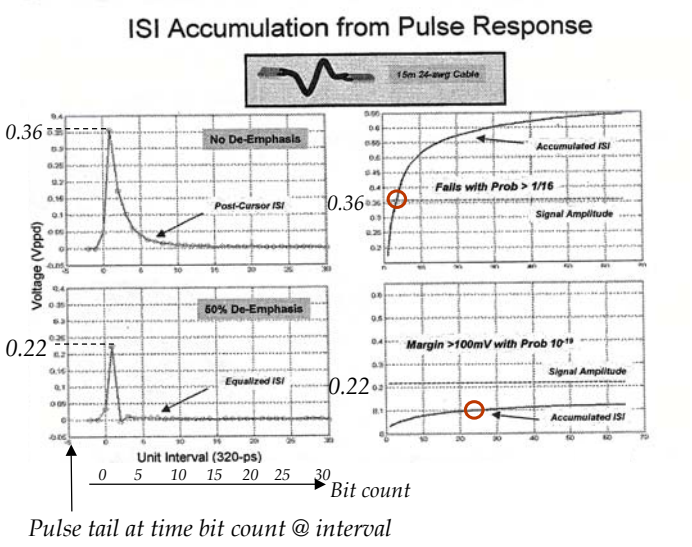


Eye for random data with maximum run length of 7.

Effect of Channel Equalization



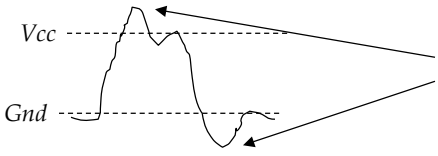
Bit Error Rate Estimation



Synchronous Design

- Synchronize Asynchronous signals ASAP
  - Put through several flip-flops in sequence
  - Use active low control signals (e.g. $\overline{\text{Reset}}$)
    - As $NM_H > NM_L$

- Overshoot matters (porches on rising edge can matter too)



Can:
- Reprogram logic
- Turn on parasitic diodes
- Reduce long term reliability
  - (injected gate current)