Design Alternatives

Timing Scenarios (Clocking strategy)

- Master synchronized clock
- Source synchronous clocking
- Clock Recovery

Basis for Signaling Circuit

- Voltage Mode vs. Current Mode
- Single sided vs. Single sided against reference vs. Differential

Termination

- Source vs. Load vs. On-chip

Direction

- Single direction vs. Bidirectional

Data Representation

- Non Return to Zero vs. Return to Zero vs. Pulse vs. N of M Code (e.g. 8b/10b)
- Pulse Amplitude Modulation : PAM-2 (binary) vs. PAM-4 (4-level)

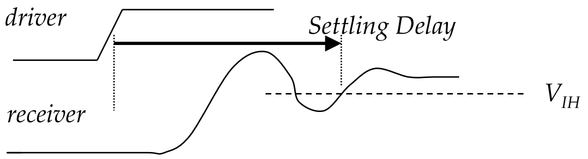
Use of Channel Compensation

Use of Error Correcting Codes

Case Study – AC-Coupled Interconenct (ACI)

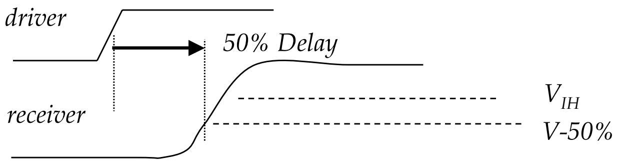
Timing Scenarios

- Sufficient delay slack for noise to settle:



  - If $t_{interconnect\text{-}max} < 5 \times$ *line delay*, then design is very simple.

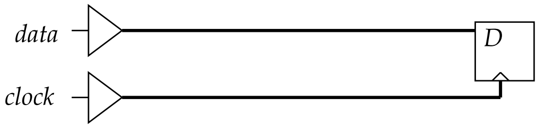
- First Incident Switching:



…Timing Scenarios

Source-Synchronous Switching

- Send clock with data
    - (or recover clock from data)



- In such systems, the rise-times and skew from inter-symbol noise, processing and temperature variations determines maximum signal speeds

E.g. 1 Gbps, 30 inch wire

t_symbol =

t_wire =

If clock jitter has to be less than 10% of t_symbol, t_jitter =

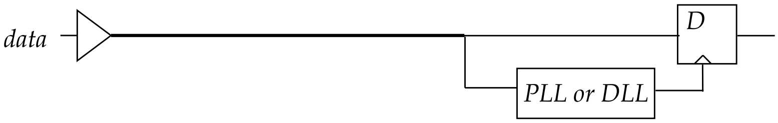
What % variation in clock “t_wire” would be acceptable?

If a via C_L = 1 pF, Z0 = 50 Ohm, what is the τ of a via?

… Timing Scenarios

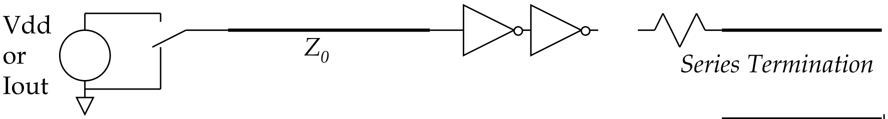
Clock & Data Recovery

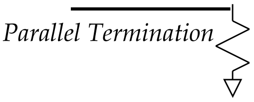
- Recover clock from the data so that delay does not need to be precisely controlled.



- Issues:
  - Ensuring enough edges in data signal to generate clock
  - Design of clock recovery circuit (Phase Locked Loop, Delay Locked Loop)

Voltage vs. Current Signalling





- RX sensitivity 300 mV
  - Vout = A Vin enough to provide full swing at O/P
- Energy per transition, Esw = $\Delta V^2 t\_line/Z_0 = \Delta I^2 t\_line Z_0$

Comparison: (Ignore lines losses)

Voltage Mode, Series Termination

Voltage Mode, Parallel Termination

Voltage vs. Current Mode

(ie. Portion of constant current source fed onto line)

Current Mode, series termination

- Requires current-mode RX (I.e. Low input impedance)

Current mode, parallel termination

- Line swing and power:

$Vsw=Z_0Iout$ $Esw= Isw^2t\_lineZ_0$

- RX swing

$Vsw=Rterm\ Iout$

In a 50 Ohm system, 300 mV requires Iout=6 mA

Sample Comparison (1 ns line)

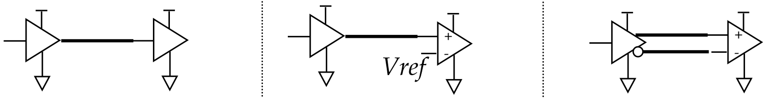
	Voltage mode, 3.3 V, series term	Current mode, 10 mA, parallel term
Esw:		

Single sided vs. Differential

Cost:

- Full differential doubles board real-estate, and pin-count

Performance



Sensitivity: Smallest RX input to give full swing at output (limited by gain A)

Noise:

TX:

RX:

Termination

Parallel vs. Series

- See above

Off-chip vs. On-chip

- High-speed requires on-chip

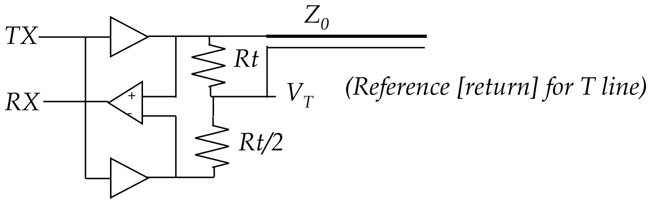
No additional reflection noise due to package delay

- How?
    - See earlier slides on resistive load
    - Common approach: Use trimming resistors and measure against an off-chip comparison

BiDirectional Signalling

Halves number of wires and pins!

Current Mode:



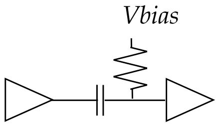
- Estimates Vtransmit from TX and substracts it from signal at pin
- Speed limited compared with single sided as estimate is imperfect (due to package, Rterm mismatch, etc.) and ISI tends to be larger
- Voltage mode and differential versions

Signal Coding

- Run length constrained and DC balanced codes
- Error Correction Coding
  - Not used much today but likely in future
- Pulse Amplitude Modulation (PAM), NRZ vs. RZ

Reasons to constrain max # and ratio of 1's or 0's

- AC Coupled Signals



Want : Fixed Vbias
➔*Average value of input signal must be known*
➔*Known ratio of 0's to 1's*
➔*AC balanced signals*

- Provide sufficient edges for clock recovery
  - ➔ Max # of 1's or 0's in sequence known
- Reduce SSN, return current and d/dt(return current)
  - ➔ Balance 01 and 10 simultaneous transitions in a bus

Concepts in Balanced Codes

Run Length

- Max # of 1's in sequence = rmax
- Min # of 1's in sequence = rmin
- Code referred to as (rmin-1, rmax-1) code

Bit Stuffing

- Simplest way to achieve a (0,m) code is to insert a false bit when rmax hit
- Requires synchronization at frame level and counters at RX and TX
- E.g. Achieving (0,2)
  - Data : 01000011110
  - Encoded data: $01000\underline{1}01111\underline{0}10$
- Though reduces low frequency content, does not eliminate a DC bias drift
- Can not predict actual symbol rate
  - Can predict worst case symbol rate
    - What is it for (0,2)?

… Concepts

Disparity

- = # of 1’s - # of 0’s

Digital-Sum Variation (DSV)

- = Max. variation in disparity
- Constant DSV ➔ DC-balanced signal, rmax = DSV
- Determines low frequency components of signal

Block Codes

Nonoverlapping Block Codes

- Each block of n bits is coded as m bits with equal numbers of 1s and 0s
- Number of zero-disparity code words in m bits is $(^{m}{}_{n/2})$
- Number of input signals is 2^n
- Thus code exists if $(^{m}{}_{n/2}) > 2^n$
- Code efficiency = n/m
- E.g. n=2, m=4

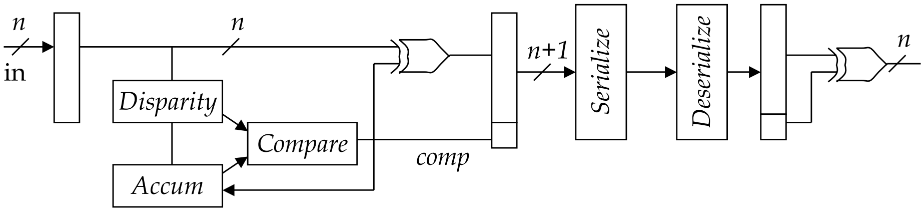
input	*code*
00	*0101*
01	*1010*
11	*1100*
10	*0011*

Efficiency = *50%*

- E.g. n = 8, m=12, efficiency = 67%

Running Disparity Codes

- Permits non-zero disparity in "code word"
- Constrains worst case disparity



- Disparity = disparity of current block
- Accum = accumulated disparity, including comp bit
- Compare = 1 if Disparity and Accum have same signs
  = ~(sign(accum)) if disparity = 0
- Max run length = 2(n+1); Disparity ranges over [-3n/2, 3n/2]
- DSV = 3n
- 8-bit burst error occurs whenever comp bit wrong

Spatial N of M Signalling

Used to reduce Common Mode noise in power/ground/return system

- Reduces SSN at TX
- Reduces signal return current
- e.g. Hamming Codes

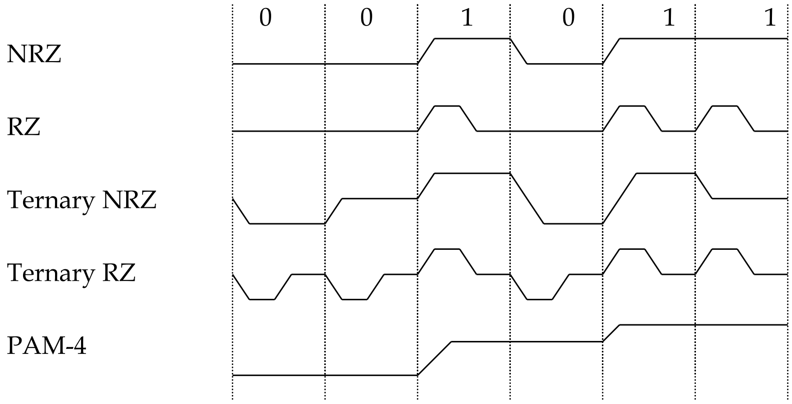
Single Symbol Encoding

NRZ = Non Return to Zero

RZ = Return to Zero

Ternary ➔ 3 level signaling

PAM-4 ➔ Encode bit pair (symbol) as one of 4 levels



Symbol Encoding Tradeoffs

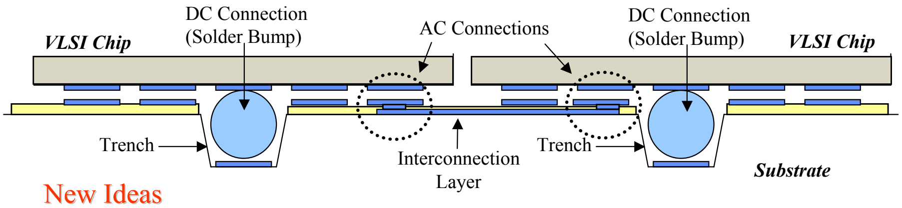
- NRZ (also called PAM-2)
  - Most common
- RZ
  - Requires 2* channel bandwidth of NRZ
  - (Only used in optical signals where BW is almost inifinite)
- Ternary NRZ
  - Use against Vref in single-sided TX, differential RX
- Ternary RZ
  - DC balanced
  - Use against Vref in single-sided TX, differential RX
- PAM-4
  - Requires half channel BW of PAM-2
  - Reduced signal swing per symbol
  - Requires ADC at RX
  - Not useful unless channel BW very limited

Case Study

AC Coupled Interconnect

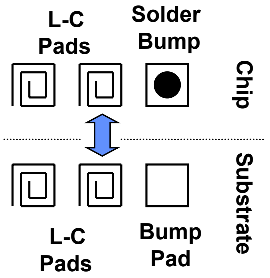
- NCSU Research Project
- Coding issues
- Eye evaluation
- Outline
  - Overview
  - Benefits
  - System view
  - Circuits
  - Eye Diagram analysis

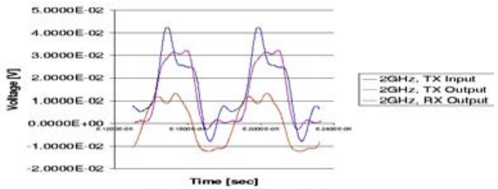
AC Coupled Interconnect Concept



New Ideas

- AC coupled connections down to 70 µm pitch
- Short- or long-range capacitive or inductive coupling
- Buried solder bumps to bring chips into proximity
- High-speed, low-power current switching techniques

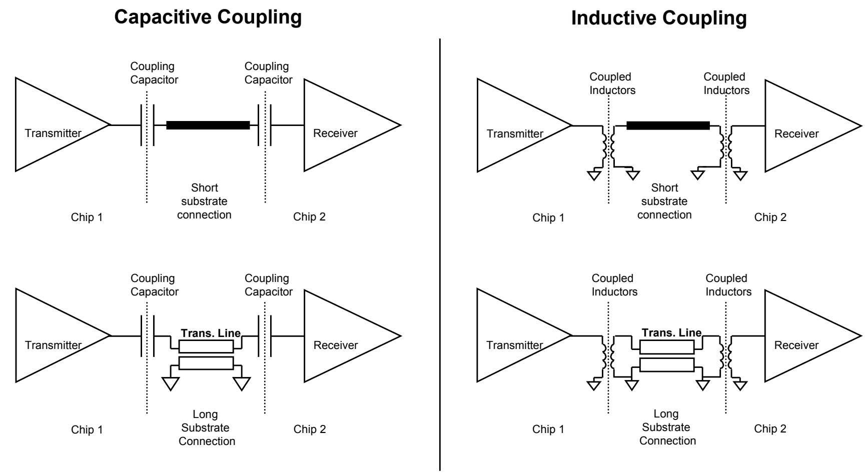




(100:1 high-Z probe)

1. Want to AC couple signals but maintain DC connections
2. Need AC pads close to substrate
3. Buried solder bumps enable both
4. Inductive or Capacitive coupling

Basic Circuit Models



Driver is simple cascaded inverter stage

Center pad chip1 to center pad chip2 -> Ccouple=21fF

pad to pad parastic -> Cparasitic=2.4fF

pad to chip ground -> Cshunt=2.5fF

This assumes no metal underneath the pads

Chip to Chip spacing is zero, but pad to pad spacing is 3.4um

- this is due to the thickness of each chip’s passivation layers

Benefits of ACI

Dense I/O

- e.g. 800 power/ground, 6,000 signal per.sq.cm.
- Achieve end of the ITRS today!
- Can be applied to dense connectors too

Low power

- 20% Transmit power of conventional interconnect

High Speed

- Will extend high speed SerDes

Robust

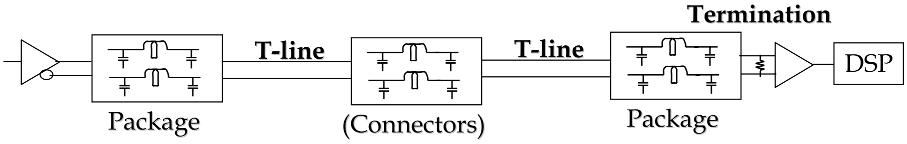
- Can achieve low Bit Error Rates

Manufacturable

- Conformable
- No change to base fabrication process and materials

System View of Conventional I/O

Typical : ~3 Gbps, 100 mW/channel link



Lossy Channel:

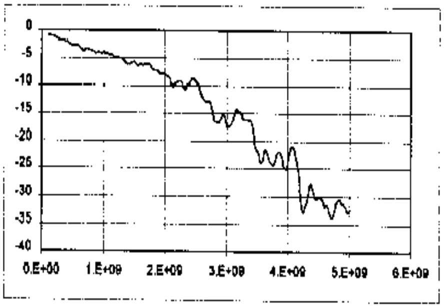
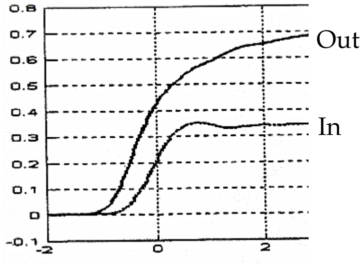


Figure 3 – Typical S21, transmission plot for serial link

d picture of what is happening in the frequency domain

DSP to sharpen edge response:



Conventional I/O

1 V in, 50-100 mV needed at RX

- Losses < 23 dB required

Low-pass filter

- Makes 10 Gbps, 20 Gbps etc. increasingly difficult

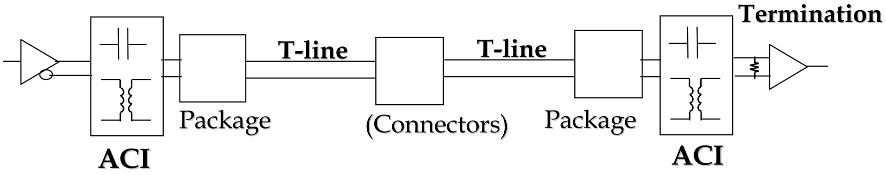
Energy per bit

- $E = \Delta V^2 t / Z_0$ + overhead for circuits & DSP
- Increased by differential, analog DSP at RX

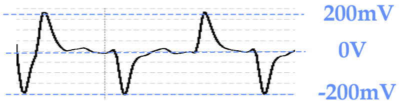
Pin-in-hole connectors

- Creates dense via field
    - Disrupts return current
    - Increases high frequency losses

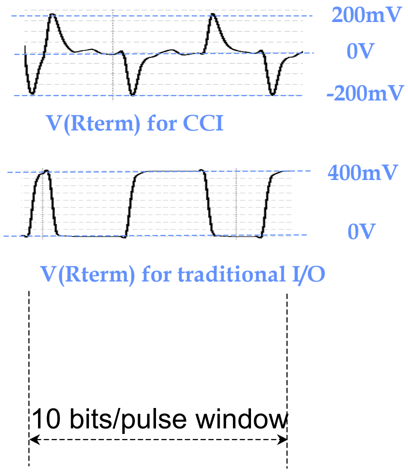
ACI



- **ACI acts as a differentiator:**
  - Pulse signaling
  - Energy per bit reduced
  - Integrate at Receiver
- **ACI acts as a high-pass filter**
  - Compensate for line losses
  - Extends useful frequency range
  - Potentially avoids DSP
- **ACI transformers can be asymetric**
  - Can accept higher line losses



Why 80% less power dissipation?



Suppose Vpp=0.4v, R=50ohm, 6Gbps

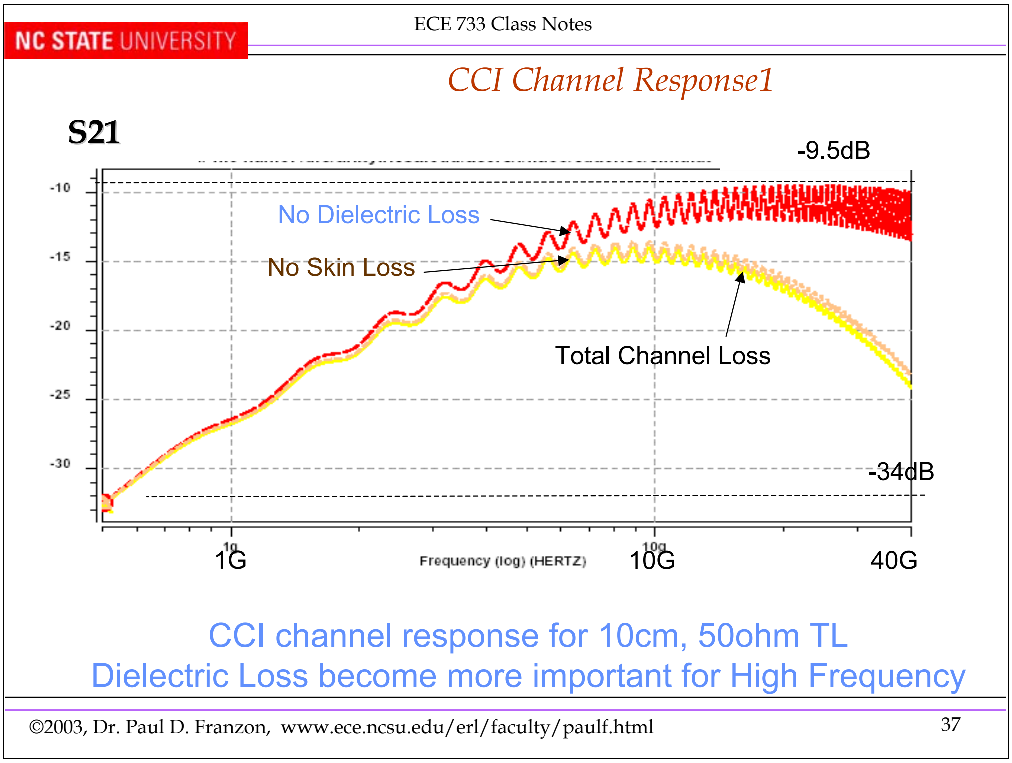
For CCI: Power of each pulse is less than (0.5*(0.2)^2/50)=0.4mw, totally 5 pulses in period of 10 pulse window, so average power is 0.2mW

For Traditional: Power of each ‘1’ bit is (0.4)^2/50=3.2mW, totally 5 ’1’bit in period of 10 bit window, so average power is 1.6W

0.2/1.6=0.125, that is 87.5% less power

For lower frequency switching, even more power saving

<< Back



ECE 733 Class Notes

NC STATE UNIVERSITY

CCI Channel Response1

S21

CCI channel response for 10cm, 50ohm TL
Dielectric Loss become more important for High Frequency

©2003, Dr. Paul D. Franzon, www.ece.ncsu.edu/erl/faculty/paulf.html

Signal Source : 1 V------Yes

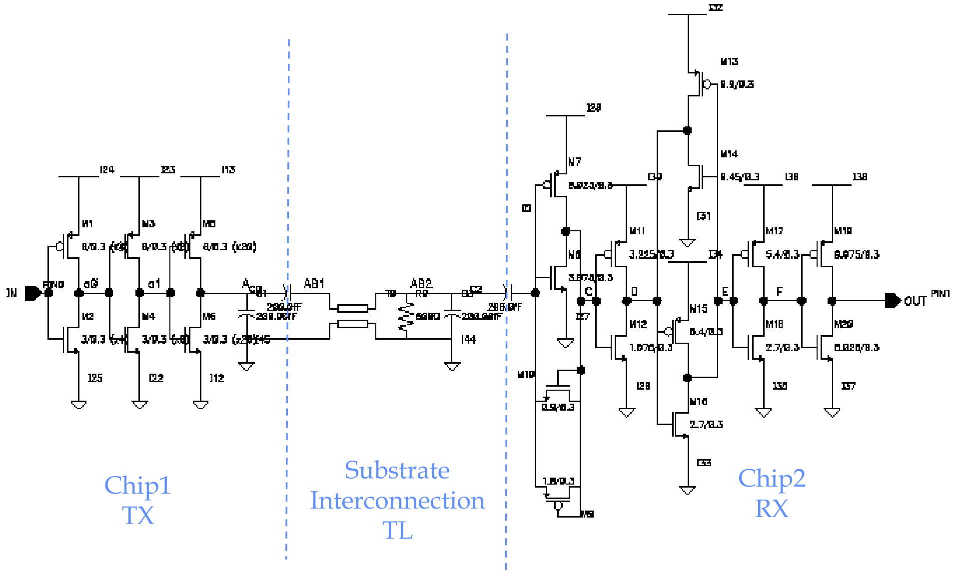
Get into dB too., 9 dB at 1 GHz. --------Now in dB, but why 9 dB at 1GHz????

REDO to just channel response w/- termination artificialities (LL)----------I am simulating what exactly in my design(no termination at RX side, so there is ripples) See backup slides: Wondering: Use Channel_out/IN or Channel_out/Channel_in???

Include sketch of ckt (LL).--------See backup slides

Include measured S12 for capacitor (KC) (or see TEAM report)—included, see next slide

CCI Circuit Schematic

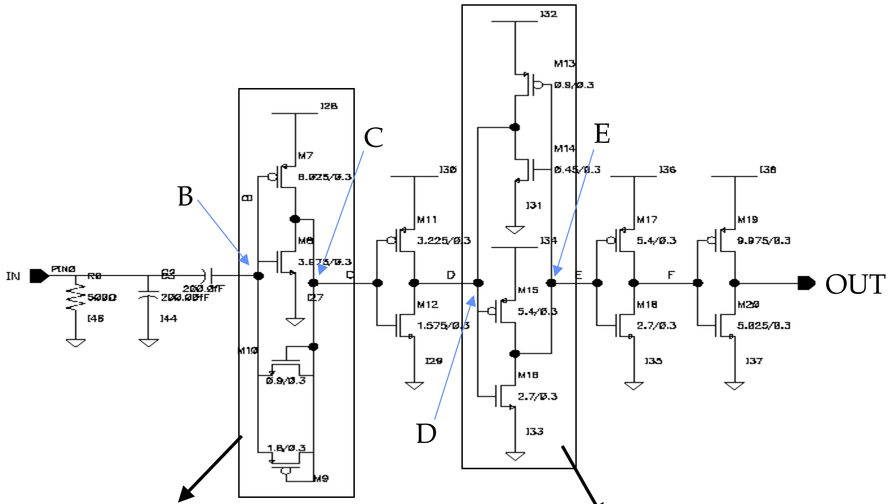


Chip1
TX

Substrate
Interconnection
TL

Chip2
RX

Kühn’s Receiver



Diode Feedback to Set up Local DC level and inhibit unwanted switching due to high frequency noise

Using Latch to recover data

Always high gain.-----added in next slide

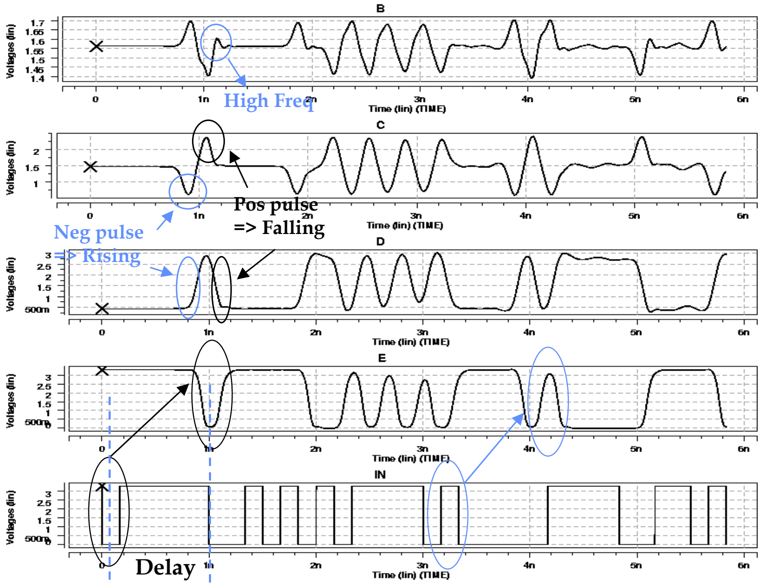
Always high Zin? Cm??----see next slide

Noise filter like calmp diode.-----see next slide

Look at freuency response and DC response.-----next slide

What does eye look like at input and why is it opening up?

How Kühn's RX Works?



High Freq

Neg pulse => Rising

Pos pulse => Falling

Delay 920ps

B

Filter out High Freq Noise

C

Recover Data by Latch

D

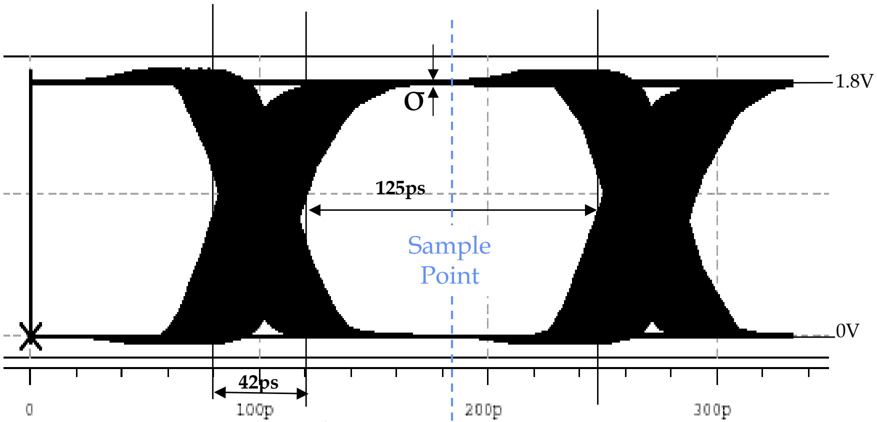
Buffer

E

INPUT

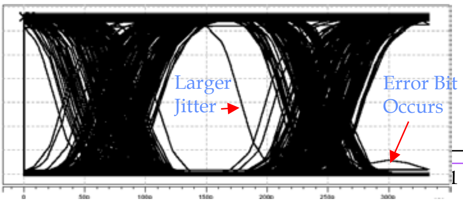
Not really high freq. noise?—see previous slide

EYE Diagram Analysis



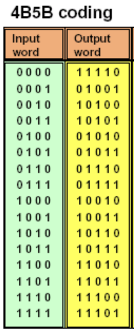
4b/5b Coding

5b/6b Coding



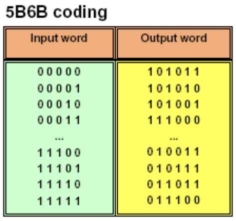
Use this signal for CDR, not input voltage.-----mentioned in slide18

Codes Evaluated



4B5B coding

Input word	Output word
0000	11110
0001	01001
0010	10100
0011	10101
0100	01010
0101	01011
0110	01110
0111	01111
1000	10010
1001	10011
1010	10110
1011	10111
1100	11010
1101	11011
1110	11100
1111	11101

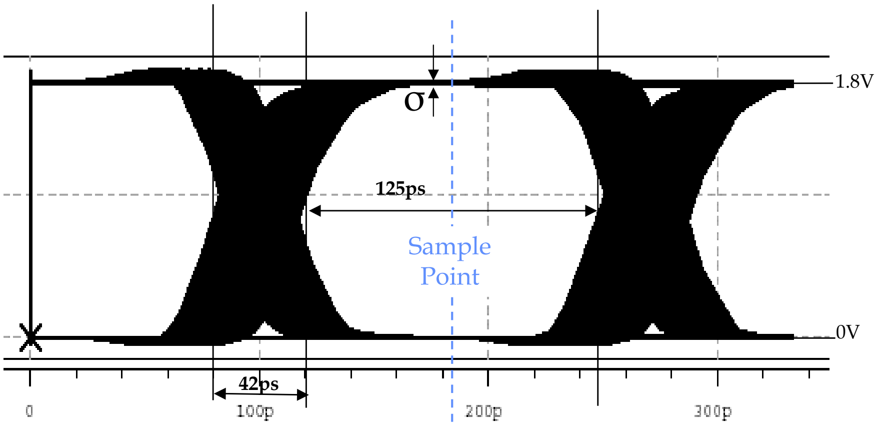


5B6B coding

Input word	Output word
00000	101011
00001	101010
00010	101001
00011	111000
...	...
11100	010011
11101	010111
11110	011011
11111	011100

Block versions.
Above, actually used a "running" version.

EYE Diagram Analysis



Highest data rate is determined by Jitter and Rising/Falling edge.

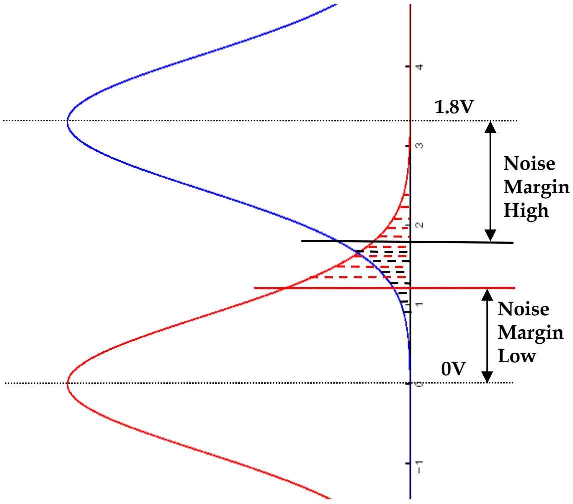
Jitter: Caused by ISI, from both coupling cap and Kuhn's Rx.

Rising & Falling Edge: Determined by Vdd, Device (R & C).

BER: Determined by EYE Opening, jitter of sample clock.

Use this signal for CDR, not input voltage.-----mentioned in slide18

Estimate BER by EYE



Note: Here we assume the signal is gauss distributed.

BER is expressed here by the shadow area:

Blue shadow for BER of ‘1’
Red shadow for BER of ‘0’

BER=Integration of the shadow area

$$BER = \int_{NMH}^{\infty} \frac{1}{\sigma_1\sqrt{2\pi}} \cdot \exp(-\frac{x^2}{2\sigma_1{}^2})dx + \int_{NML}^{\infty} \frac{1}{\sigma_0\sqrt{2\pi}} \cdot \exp(-\frac{x^2}{2\sigma_0{}^2})dx$$

$$= \frac{1}{2} erfc(\frac{NMH}{\sqrt{2}\sigma_1}) + \frac{1}{2} erfc(\frac{NML}{\sqrt{2}\sigma_0})$$

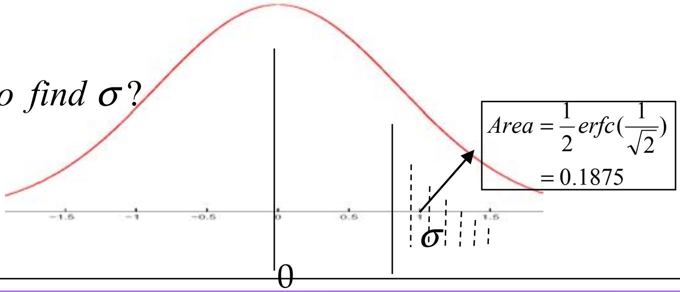
$$if\ \sigma_0 = \sigma_1 = \sigma, NMH = NML = 0.6V,$$

$$BER = erfc(\frac{NM}{\sqrt{2}\sigma}) \le 10^{-12} \quad \Leftrightarrow \quad \sigma = \frac{NM}{7} \le 0.085V$$

$$BER = erfc(\frac{NM}{\sqrt{2}\sigma}) \le 10^{-17} \quad \Leftrightarrow \quad \sigma = \frac{NM}{8.6} \le 0.07V$$

How to find σ?

Note: Here we assume the signal is gauss distributed.



$$Area = \frac{1}{2} erfc(\frac{1}{\sqrt{2}})$$
$$= 0.1875$$

Redo to get 10-17. What NM gives 10-17??----added

Schmidt Trigger RX.-------what do you mean?????

Summary

What are the main factor(s) that cause eye closure?

How is equalization useful?

How are current mode and voltage mode signalling different?

What are the advantages of single-sided TX, differential RX over single-sided RX?

… Summary

What is the advantage of a full differential system?

What are the uses of DC-balanced and run-length codes?

What is the potential advantage of PAM-4 over PAM-2?