

Static Circuits

Static Circuits

- CMOS Inverter
 - Analysis
 - ◆ Static (Transfer Characteristic)
 - ◆ Dynamic (Transient Response)
 - Driving large loads
- Logic Gates
- Pass and Transmission Gates, high-Z gates
- Latches & Flip-Flops
- Power and Energy-Delay

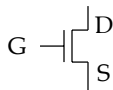
CMOS Circuit Analysis

Basic Principles:

Analysis of any digital circuit usually revolves around determining the transistor states for each region of operation.

- Basic Approach :
1. Estimate states or voltages
 2. Calculate voltages or states
 3. Make sure self-consistent

<u>Region</u>	<u>State</u>	<u>Equivalent Circuit</u>
$ V_{GS} < V_T $	OFF	
$ V_{GS} - V_T > V_{DS} \geq 0$	LINEAR	(Resistor)
$V_{DS} \geq V_{GS} - V_T \geq 0$	SATURATION	(Constant Current Source)



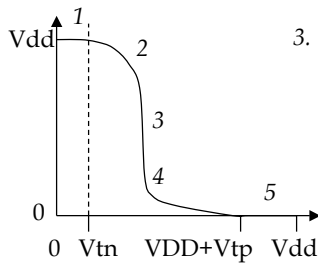
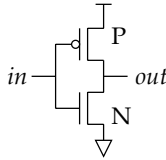
Source of "majority carriers"
(e- in nmos case, p+ in pmos)

CMOS Inverter

Static CMOS Inverter:

To simplify, use $V_{dd}=3.3\text{ V}$
 $|V_T| = 0.5\text{ V}$ in examples

- Transfer Characteristic:



- 1 : $V_{in} = 0, V_{out} = V_{dd}$
 N: $V_{GS}=0, V_{DS}= 3.3, |V_{GS}| < |V_T|$: Off
 P : $V_{GS}=3.3, V_{DS}=0, |V_{GS}-V_T| > V_{DS}$: LINEAR
- 2 : $V_{in} > |V_T|$
 N: $V_{GS}\sim 1, V_{DS}\sim 3, V_{DS} \geq |V_{GS}-V_T|$: SATN
 P : $V_{GS}\sim 3, V_{DS}\sim 0.3, |V_{GS}-V_T| > V_{DS}$: LINEAR
3. $V_{in} \sim V_{out}$
 N: $V_{GS}\sim 1.6, V_{DS}\sim 1.6, V_{DS} \geq |V_{GS}-V_T|$: SATN
 P : $V_{GS}\sim 1.6, V_{DS}\sim 1.6, V_{DS} \geq |V_{GS}-V_T|$: SATN
 4 : N : LINEAR; P : SATN
 5 : N : LINEAR; P : OFF

CMOS Inverter

“Trip” Voltage

- where $V_{out} = 0.5\text{ VDD}$
 - ♦ Both nFET and pFET in saturation

Trip Voltage changes with β and V_t
 •Esp. W/L

$$I_{DSn} = -I_{DSp}$$

$$\frac{\beta_n}{2}(V_{in} - V_{Tn})^2 = -\frac{\beta_p}{2}(V_{in} - V_{DD} - V_{Tp})^2$$

$$V_{in} = \frac{V_{DD} + V_{tp} + V_m \sqrt{\beta_n / \beta_p}}{1 + \sqrt{\beta_n / \beta_p}}$$

- If $\beta_n = \beta_p$ and $V_{tn} = -V_{tp}$, $V_{in} = V_{DD}/2$ (1.65 V with parameters on prev. page)
- What if $k_n = 2k_p$, $W_n/L_n = W_p/L_p$, $V_{DD} = 3.3$, $V_{tn} = -V_{tp} = 0.5$?

CMOS Inverter

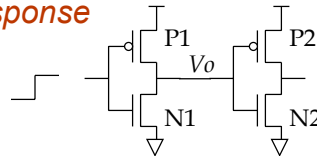
Trip voltage moves with W/L

- Would you expect V_{IL} , etc. to move with W/L?

How would you design an inverting receiver where input high noise and low noise have approx. equal magnitudes?

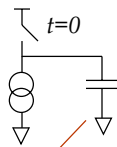
Transient (Step) Response

Ideal Fall Time:



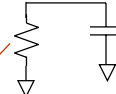
Equivalent Circuit:

$$V_o \geq V_{DD} - V_{tn}$$



Linear Discharge

$$V_o < V_{DD} - V_{tn}$$

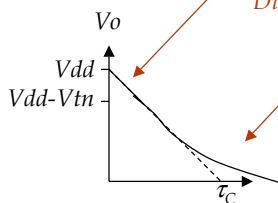


90% - 10% Fall Time

$$C_L \frac{dV_o}{dt} + I_{DS} = 0$$

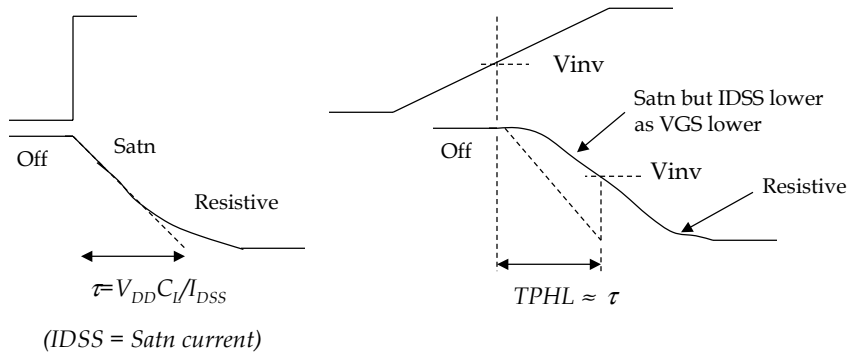
$$t_f = C_L \int_{V_{DD}-V_{tn}}^{0.9V_{DD}} I_{DS}(sat) dV_o + \int_{0.9V_{DD}}^{V_{DD}-V_{tn}} I_{DS}(linear) dV_o$$

$$t_f \approx 4 \frac{C_L}{\beta_n V_{DD}}$$



Constant Current Approximation

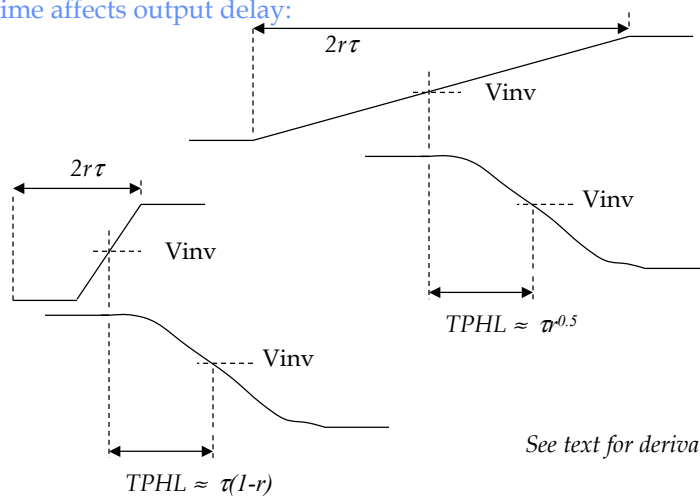
Step response vs. response to input with rise time = output fall time



See text for "derivation"

Constant Current – Rise Time

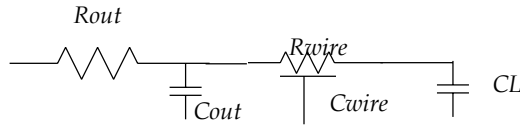
Input rise time affects output delay:



See text for derivation.

Linear Resistor Approximation

Most useful when dealing with wire resistance or transmission gate resistance



$$\tau_{rise} \approx 2.2 R_{out} (C_{out} + C_{wire} + C_L) + 0.9 R_{wire} C_{wire} + 2.2 R_{wire} C_L$$

$$\tau_{delay} \approx 0.7 R_{out}(C_{out}+C_{wire}+C_L) + 0.4 R_{wire}C_{wire} + 0.7 R_{wire} C_L$$

Source : Bakoglu, "Circuits Interconnections and Packaging for VLSI" (Addison-Wesley)

Example

Minimum size gates in 0.35 μm process

$$\begin{aligned} C_L &= 2 * \text{Drain capacitance} + 2 * \text{gate capacitance} && (\text{assuming nFET, pFET} \\ &= 2 * 0.9 + 2 * 1 \text{ fF} && \text{same drain capacitance}) \\ &= 3.8 \text{ fF} \end{aligned}$$

$$I_{DSS} = 2 \text{ mA}$$

$$R_{out} = 708 \text{ } \Omega$$

Constant current source method

$$\text{Delay} \approx \tau \approx V_{DD} C_L / I_{DSS} = 3.3 * 3.8E-15 / 2E-3 = 6 \text{ ps}$$

Resistance approximation

$$\text{Delay} \approx 0.7 R_{out} C_L = 0.7 * 708 * 3.8E-15 = 2 \text{ ps}$$

- Constant current source method closer for circuits with short wires
- In any case, these methods are mainly used for comparison in design, rather than exact prediction

FO-4

Delay increases with fan-out due to extra gate loading

Common metric to evaluate a high-speed CMOS process is FO-4

- Delay of a minimum size inverter with a fan-out of 4
- About equal to delay of 2-input 2-output logic gate
- Ex. Using constant current method

$$\begin{aligned} CL &= 2 * \text{Drain capacitance} + 8 * \text{gate capacitance} \\ &= 2 * 0.9 + 8 * 1 \text{ fF} \\ &= 9.8 \text{ fF} \end{aligned}$$

$$\text{Delay} \approx \tau \approx V_{DD} C_L / I_{DSS} = 3.3 * 9.8 \text{E-15} / 2\text{E-3} = 16 \text{ ps}$$

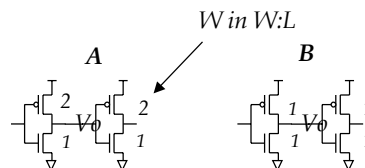
(This is actually an under-estimate as normally the PFET would be larger, increasing the fall time and v_{sat} was ignored).

Transistor Sizing

In this 0.35 mm process:

- $\mu_n = 4 \mu_p \rightarrow \beta_n = 4 \beta_p \rightarrow \text{trise} = 4 \text{ tfall}$
 - ♦ Undesirable!
- Thus W_p is usually larger than W_n
- Accounting for velocity saturation $W_p : W_n = 2 : 1$ normally gives about equal rise and fall times
 - Also gives reasonable V_{inv}

Which has the slower falling edge at V_o :

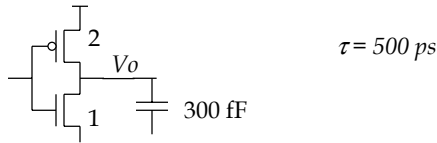


- Sometimes one edge matters more than another, and transistors might be not designed at 2:1
 - ♦ At the expense of V_{inv} and NM though

Driving Large Loads

Series ratio'd drivers used to drive large loads:

- Driving large load with small driver, very slow



- So, need larger driver
- But larger driver itself has to be driven (and has a high C_{in})
- **Solution:**
 - A string of increasing size drivers
 - Optimum sizing if each stage increases by approximately 3 - 4 over previous stage

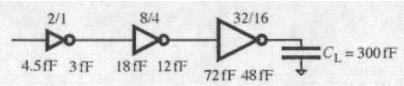


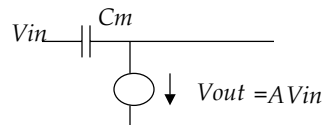
FIGURE 4-35 An Exponential Horn

Miller Effect Capacitance

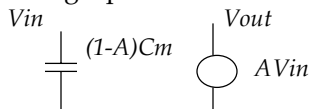
Affects capacitance seen by small-signal equivalent circuit.

Miller's Theorem:

Series capacitance in gain ckt:



Can be transformed to the following equivalent circuit:



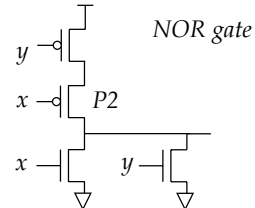
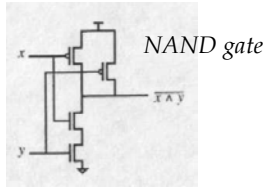
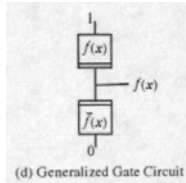
A is -ve → C_{in} increases a lot in high gain region (at V_{in})

→ $Z_{in} = 1/j\omega C_{in}$ changes a lot in this region

▲ Matters when constant known Z_{in} matters

Static Logic Gates

Complementary pull-down and pull-up circuits



Analysis & Design Issues

- Body Effect changing V_{tn} for upper pull-up
- Transistor sizing:
 - Can speed up one path over another. (Note : Body effect on P2)
 E.g. If path through 'x' is more critical, increase those transistors sizes.
 If 'y' had to be faster (input arrived later in clock cycle) would it make sense to swap y with x?

Complex Static Gates

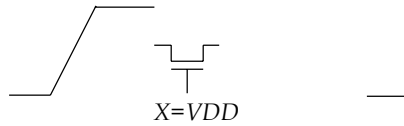
Design AND-OR gate:

$$F = AC + BD$$

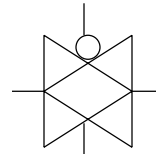
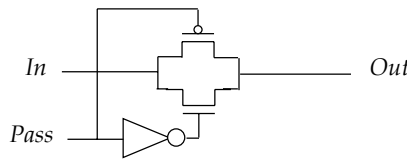
Transmission Gates

Pass Gates:

- What is the limitation of an n-type pass gate?



- Fix with a transmission gate:



Use for:

- Logic, esp. muxes
- Bi-directional structures
- E.g. Segmented buses

Latches & Flip-flops

Basic Latch:

- Latch event on falling edge of clock

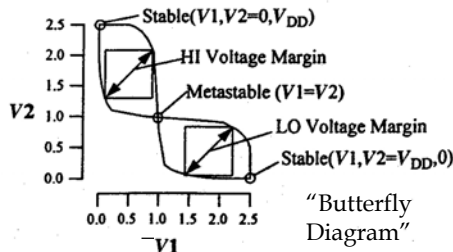
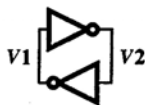
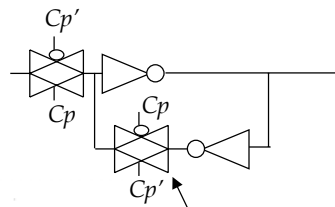
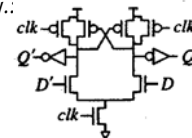


FIGURE 12-4 Cross-Coupled Inverter Steady-State Conditions



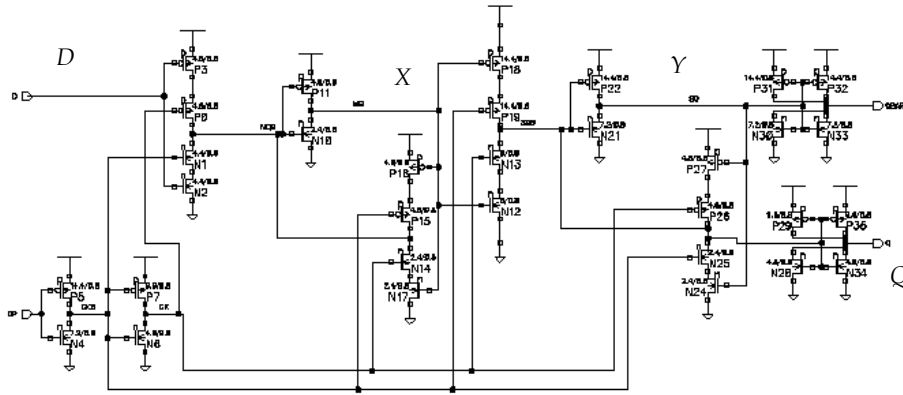
Breaks feedback (regeneration) to program Latch.
Alternative: Overpower directly.



(a) CVSL Latch

Edge Triggered Flip Flop

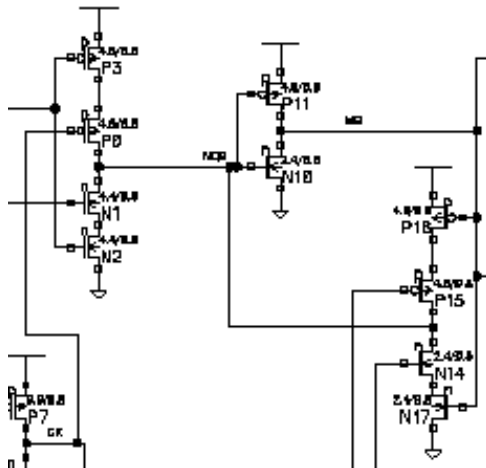
Taken from CMOSX 0.8 um cell library



Note "overdesign": - clock rebuffering
 - extra drive circuits

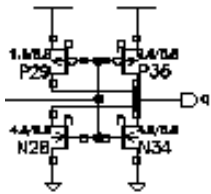
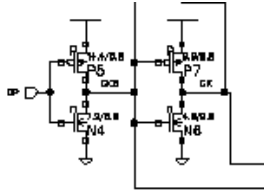
Detail

Draw equiv. Ckt.



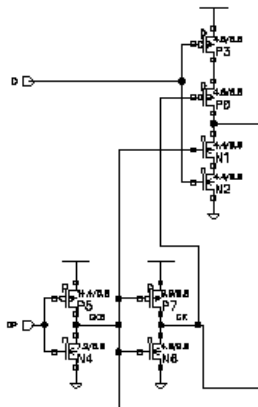
Standard Cell

Note "over design" features



Circuit

What else would this circuit be useful for?



Differential Edge-Triggered Flip-flop

"Strong Arm" Flip-flop

- Single-phase, edge triggered
- Slave is clocked by the master
- Analyzed separately

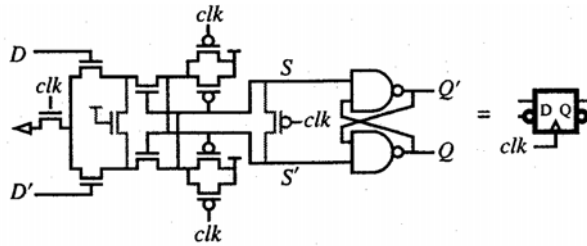


FIGURE 12-16 Differential Edge-Triggered Flip-Flop

Flip-Flop Failure Mechanisms

Set-up and Hold

- Determined by delays in circuit
- Hold violation can occur if signal can race through both stages of a static edge triggered F/F
 - Not clock' was delayed w.r.t. clock
 - ♦ This could lead to race-through

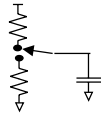
Clock Slope

- Slow clock edges can result in race-through

Power Consumption of Static Gates

Static CMOS Gate power consumption:

- Almost 0 power consumption when in 0 or 1 state
 - Except for sub-threshold and leakage current
- When switching:



+ brief short-circuit current during switching event.

- When $V_{out} 0 \rightarrow 1$:
$$E = \int_0^{V_{dd}} (V_{dd} - V_{out}) Idt = \int_0^{V_{dd}} (V_{dd} - V_{out}) CdV_{out} = \frac{CV_{dd}^2}{2}$$
- Complete 010 toggle : $E = CV_{dd}^2/2$
- Power consumed at each node, $P = SA f_{clock} CV_{dd}^2/2$
- Where SA = Switching Activity
 - % of clock cycles when node switches

Energy-Delay Product

Power and Speed can be traded off:

- Energy per switching event $\propto V_{dd}^2$
- Gate delay $\propto Id_{ss} = b(V_{dd} - V_T)^2$
 - I.e. $\propto V_{dd}^2$
- Power \propto energy * $f_{clock} \sim V_{dd}^4$
- Tradeoff:
 - Halve $V_{dd} \rightarrow$ Quarter speed, one-eight the power
 - (until V_{dd} starts approaching $2 V_T$, at which delay goes up rapidly)
- Why not just drop V_T ?

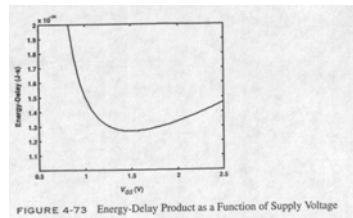


FIGURE 4-73 Energy-Delay Product as a Function of Supply Voltage

- Some chip designs, change V_{body} to permit changes in V_T and thus tradeoffs of speed and leakage power during operation

Summary

What are the steps in DC Analysis?

What are the two approaches to transient analysis?

How are pMOS sized wrt nMOS transistors?

What is the power consumed in a static CMOS circuit?