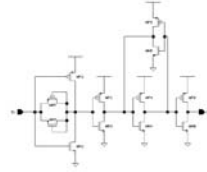


Digital Circuit Design Introduction

Dr. Paul D. Franzon



Outline

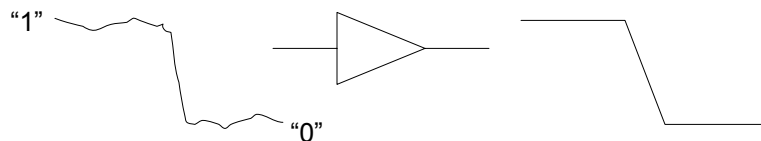
1. Digital circuit characteristics, design objectives & issues

References

- Doane & Franzon, "Multichip Module Technologies & Alternatives", CH. 11
- Hodges & Jackson, Analysis & Design of Digital Integrated Circuits
- + many other texts

Digital Circuits

Unlike Analog circuits, digital circuits reject noise
Logic restoration



Permits limitless scaling with correct "function".

How Digital Ckts reject noise

Via non-linear gain in the logic gate:

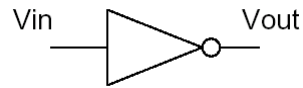
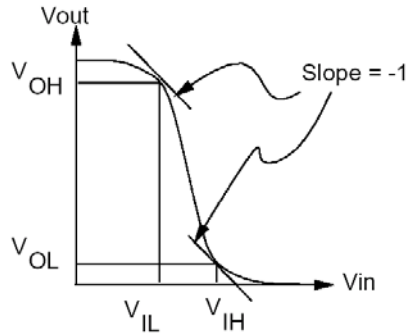
Noise Margin provided:

- V_{OL} V_{output_low}
- V_{OH} V_{output_high}
- V_{IH} V_{input_high}
- V_{IL} V_{input_low}

Define at points where transfer characteristic has unity slope

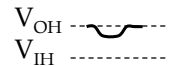
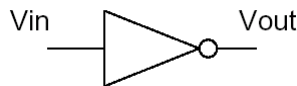
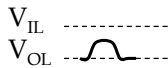
$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

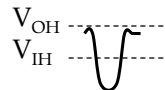
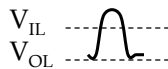


Why This Definition?

What happens in each case?



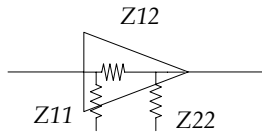
Gain < 1
Noise pulse attenuated



Gain > 1
Noise pulse amplified!
Potential Logic Error!

Input-Output Impedances

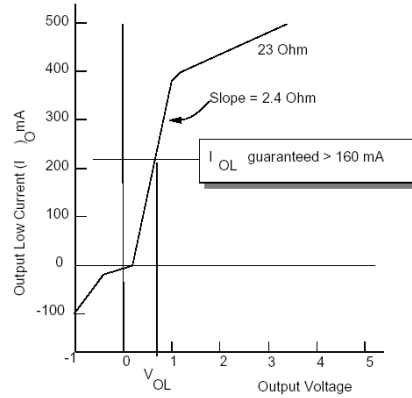
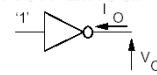
Impedances are non-linear



e.g. $Z22 = V_{out}/I_{out}$ with V_{in} open ckt

CMOS

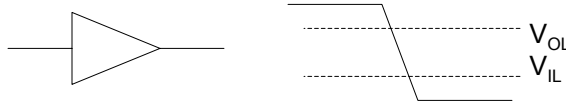
- Usually
 - Input $Z11$ is capacitive
 - Trans $Z12$ is ∞
 - Output impedance, $Z22$, is
 - ♦ RC



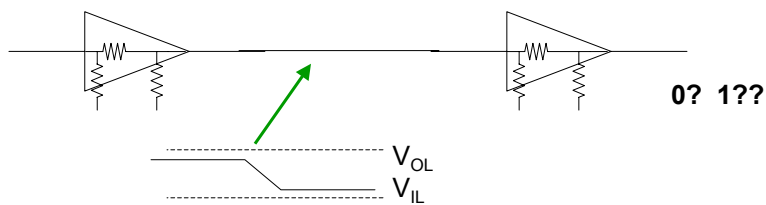
Why do impedances matter?

Some logic families have finite $Z11$, $Z12$

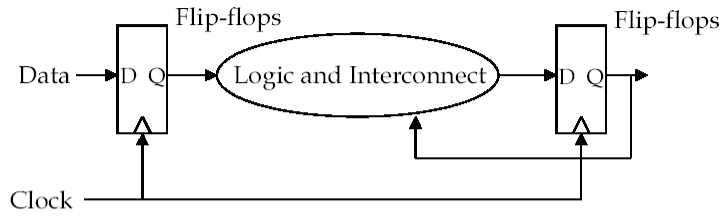
- Determines ability to support fan-out
 - Ie. Number of load gates
 - Unloaded Gate:



- Extreme example of a loaded gate:

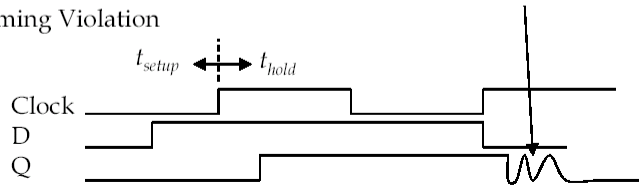


Synchronous Design



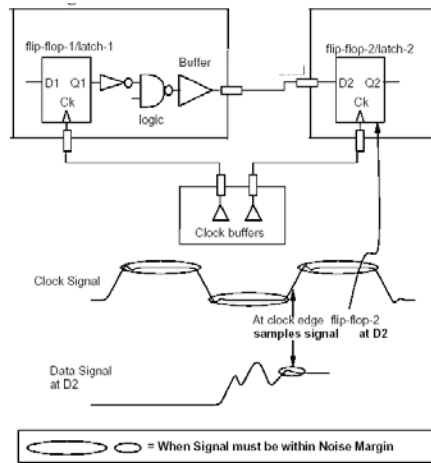
Flip-flop behavior:

- Samples input signal during set-up and hold period
- If signal changes state during set-up and hold => *Metastability*
- ◆ =Timing Violation



Signal Integrity

Signal Integrity = Controlling Delay & Noise

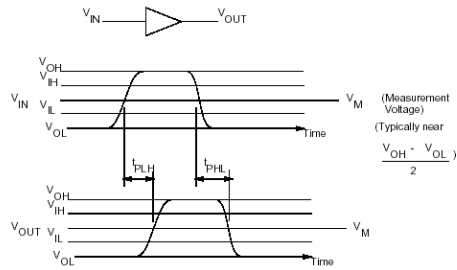


Timing Design

Timing Specifications

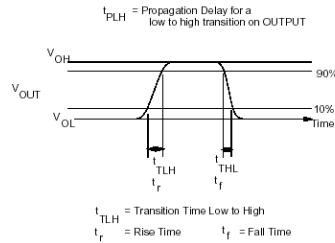
Delay

- Referenced to a single voltage
 - Usually 0.5 Vswing
 - Sometimes V_{IH} , V_{IL}
 - $t_{PLH} : 0 \rightarrow 1$ delay
 - $t_{PHL} : 1 \rightarrow 0$ delay



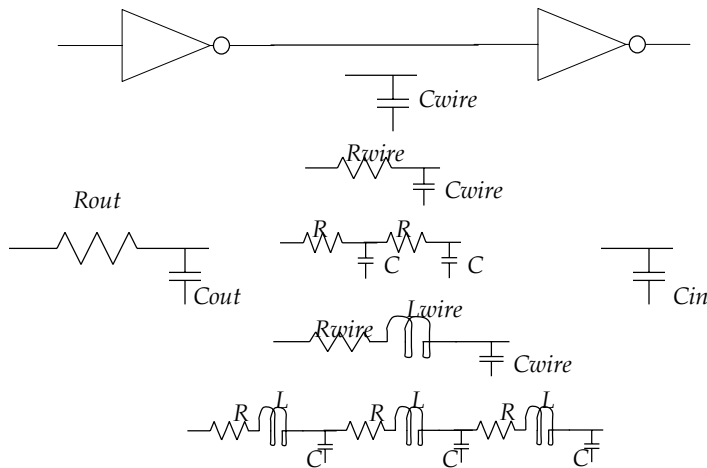
Rise Time

- Usually referenced to 0.1 & 0.9 Vswing
- t_{TLH} : Rise time
- t_{THL} : Fall time



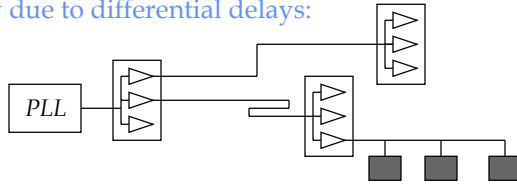
Delay

Delay can be modeled by an RLC equivalent circuit



Clock Skew

Skew due to differential delays:



- Skew = systematic variation
 - ◆ Varied buffer delays
 - ◆ Wiring delay differences

Jitter = cycle to cycle variation at any one point

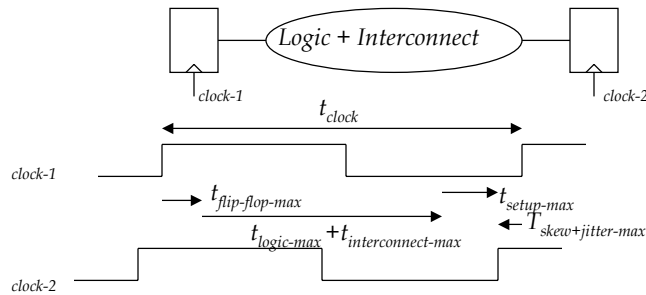
- ◆ Phase lock loop noise
 - caused by noise in Vdd/Gnd
- ◆ Varying trigger points at buffer
- ◆ Environmental effects

Timing Equations

Minimum Clock Period:

- Prevents 'setup violations'

$$t_{clock} = t_{flip-flop-max} + t_{logic-max} + t_{interconnect-max} + t_{setup-max} + t_{skew-max} + t_{jitter-max}$$



$t_{interconnect}$ refers to 'timing slacks' for interconnect.

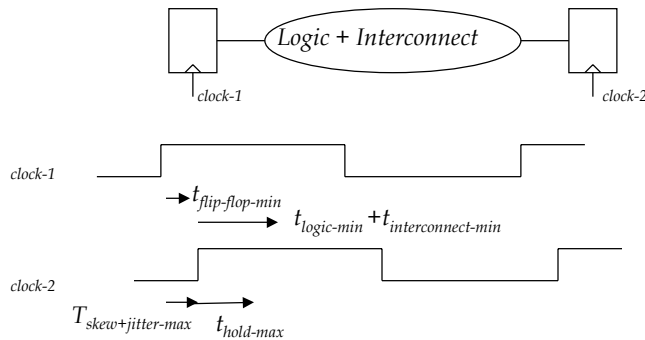
- Must be allocated amongst different noise sources using a timing budget

...Timing Equations

Requirement to Prevent Race:

- Prevents 'hold violations'

$$t_{hold-max} < t_{flip-flop-min} + t_{logic-min} + t_{skew-max} + t_{interconnect-min}$$



Sources of Noise

1. Ringing noise due to transmission line reflections or RLC resonance.
 - Signal noise mainly of concern on longer wires
2. Noise pulses due to crosstalk from switching on neighboring lines.
 - Signal noise mainly of concern on longer wires
3. Noise pulses or false signaling and sensing due to noise on power and ground system
 - Simultaneous Switching Noise
 - DC voltage drop on power supply
 - Other common mode noise
 - Usually enters through power and ground pins of circuit

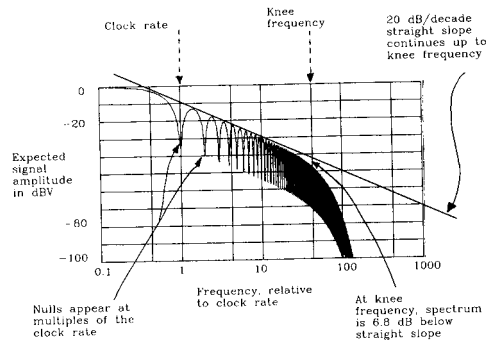
Broadband nature of digital signals

Take the Fourier Transform of a digital signal and there is a lot of high frequency energy

- The faster the rise and fall time, the more high frequency energy there is
- 3-dB bandwidth can be approximate, by assuming an equivalent RC ckt:

$$BW = 0.35 / t_r$$

- Often significant harmonics to 7-10 x BW



Summary

- Digital circuits reject noise up to the noise margin

$$\begin{aligned} V_{OL} &= 0.1 \text{ V} \\ V_{OH} &= 2.4 \text{ V} \\ V_{IL} &= 0.8 \text{ V} \\ V_{IH} &= 1.7 \text{ V} \end{aligned}$$

$$\begin{aligned} NM_H &= \\ NM_L &= \end{aligned}$$

- How is delay usually measured?
- What is metastability?
- What is the approx. 3-dB bandwidth of a 1 Gbps signal with 35 ps rise and fall times?