HIGH SPEED MULTISTAGE CMOS CLOCK BUFFERS WITH PULSE WIDTH CONTROL LOOP

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Abstract—In high speed CMOS clock buffer design, the duty cycle of clock is liable to be influenced when the clock passes through a multistage buffer because the circuit is not strictly digital. Signal quality degradation is caused by temperature and process deviation. In this paper, we address a pulse width control loop (PWCL), to get a required pulse width. To investigate the loop stability, a linearized small signal analysis model is used. Results of SPICE simulation show that the pulse width can be well controlled if the loop parameters are properly chosen. The pulse width can be easily adjusted to a desired value by changing the ratio of transistor sizes in the current mirror of the charge pump.

I. INTRODUCTION

To reach the highest circuit speed in CMOS applications, clock drivers and buffers must be carefully designed. A great deal of attention has been paid to clock recovery, clock generation, clock deskew, timing and clock distribution. Automatic control techniques, such as PLL and DLL [1]-[2], have been widely used for clock circuitry for many years. In low speed applications, PWM technique is employed to motor control, power conversion and even A/D conversion [3]-[5], but as for pulse width control in high speed clock buffer design, only a few minor feedback loops have been reported [2], [6].

In high speed design a multistage clock buffer implemented with an inverter chain is often needed to drive a heavy capacitive load, and in BiCMOS and low power designs, ECL-CMOS or other level conversion circuitry is usually required. For these designs, it is difficult to keep the clock duty cycle at 50%. When a clock signal passes through a multistage buffer, the pulse width may be changed due to the unbalance of the P and N transistors in the long buffer. This unbalance can be introduced by many factors, such as process deviations, temperature change or mismatch in design. For level conversion from low to high, circuits are more sensitive to design mismatch than in normal CMOS. In high speed applications, this becomes serious when the number of the stages is very large. As a consequence, the clock duty cycle will wander away from 50%, and in the worst case, the clock pulse may disappear inside the clock buffer as the pulse width turns to be too narrow or too wide.

In this paper, we address a new pulse width control loop (PWCL) technique, which can be used to control the pulse width in a multistage clock buffer or a level converter, or in converting sinusoid waveform to a required pulse sequence with a certain pulse width.

The PWCL is a nonlinear feedback loop, however, in order to analyses the loop behavior a linearized small signal model is suggested. Two charge pumps are used in the loop, so temperature influence and process variation will be rejected as they appear in common mode. Loop stability is discussed, and finally SPICE simulation and test chip measurements are provided.

II. LOOP CONFIGURATION

The configuration of a clock buffer with a pulse width control loop (PWCL) is shown in Fig.1(a). Without the PWCL feedback, it is a normally designed clock buffer. To investigate the behavior of the loop we model it as shown in Fig.1(b). The feedback loop functionally consists of a control stage (CS), an ideal comparator (Comp), a charge pump (CP), a loop filter (LF) and an amplifier (Amp). A pure delay unit (DU) is introduced to characterize the delay in the long inverter chain or buffer. We assume that the pulse width of the clock buffer is controllable. It means that when the pulse width of clock buffer output deviates an offset from a required duty cycle, it should be possible to adjust the control voltage so that the offset is removed. It implies that the controllable dynamic range will cover the range of possible offset. The number of stages in the clock buffer must meet a condition that negative feedback is guaranteed. In order to reduce the control power and the static current, it is preferable to choose the first stage of the clock buffer as the controlled stage.

III. LINEARIZED SMALL SIGNAL ANALYSIS

A. Idealized Clock Buffer with Control Stage

If a clock buffer chain consists of many stages, its gain is so large that even for a small signal fed into the first stage, the output of the final stage is digitized. This is modeled by the behavior of the Comp. We can imagine that there is a decision level \( V_d = V_{dd}/2 \) inside the Comp, and an input
changed at most by $tr + tf$. Out of these ranges, nonlinear properties will dominate or the loop behaves irrationally.

### B. Charge Pump

A charge pump of single end output is shown in Fig.4.(a) and (b).

As the output impedance $R_{p}$ and $R_{n}$ are not infinite, the effect of $R_{p}$ and $R_{n}$ can be viewed as a leakage of charge. In loop behavior analysis, we model the leakage impact by an equivalent resistor $R$. The average output of charge pump during one period $T_{c}$ is approximately expressed as

$$\overline{I_{c}(t)} = \frac{1}{T_{c}}[(w_{0}(h))I_{p} - w_{1}(h)I_{n}]$$

where $w_{1}(h) = w(h)$, $w_{0}(h) = T_{c} - w(h)$, $I_{n}$ and $I_{p}$ are always positive. If the PWCL is stable, the final value of $\overline{I_{c}(t)}$ will approach zero. It implies that the charge and discharge are balanced during the period $T_{c}$, and we get the balance condition as

$$w_{1}(h)I_{n} = w_{0}(h)I_{p}$$

If the currents draw from the current mirror, $I_{p}$ and $I_{n}$ are equal, then $w_{1}(h)$ will be the same as $w_{0}(h)$. Therefore, we can get a clock pulse with duty cycle 50%. By sizing the transistor widths of $M_{n}$ or $M_{p}$, we can obtain the required pulse width as long as the circuit speed allows. The sensitivity of average current against pulse width is

$$K_{v} = \frac{d\overline{I_{c}(t)}}{dw} = \frac{-(I_{n} + I_{p})}{T_{c}}$$

The PWCL needs differential signals in its amplifier inputs. Here we design two charge pumps. One of them is used for detecting pulse width of the clock being controlled and the other is connect to a standard clock with 50% duty cycle for generating bias $V_{ref}$. $V_{ref}$ is taken as the reference voltage in the amplifier $Amp$.

In practice, we employ two identical single-end charge pumps, CP1 and CP2 in Fig.4.d. CP1 controls current by the clock pulse for detecting the change of pulse width, and CP2 creates a reference $V_{ref}$ by connecting to a reference clock with 50% duty cycle. In CP1, if we change the intensities of current source $Ip$ or sink $In_{1}$, a required pulse width can be easily created according to Eq.(5).
Fig. 5. Equivalent small signal circuit of the open loop (a) and the closed-loop (b).

C. Loop Stability Condition

The open loop of PWCL is shown in Fig.5(a). We can write the open loop response for Fig.5(a) as

\[ F(s) = \frac{V_{os}(s)}{V_i(s)} = \frac{A_0}{(1 + \tau_1 s)(1 + \tau_2 s)} \]  \hspace{1cm} (7)

where \( V_{os} \) is the output of the amplifier, and

\[ A_0 = K_w K_i AR \]  \hspace{1cm} (8)

is the open loop gain, and \( \tau_1 = RC_1, \tau_2 = R_2 C_2 \). As for the case of sinusoidal input, \( A_0 \) is

\[ A_0 = \frac{2 (I_n + I_p)(t_u + t_f) AR}{\pi V_{pp}} \]  \hspace{1cm} (9)

Similarly, for the square wave input, the gain is

\[ A_0 = \frac{(I_n + I_p)(t_u + t_f) AR}{2 ST V_{pp}} \]  \hspace{1cm} (10)

Strictly speaking, \( A_0 \) is non-linear for a large input case. However, for simplicity, we use equation (9) and (10) as an approximation to analyses the loop behavior in the small signal case which determines the final status of the loop if it is a stable one.

When delay time \( t_d \) is introduced by DU, it leads to a factor \( e^{-\tau_d s} \) in the open loop transfer function \( G(s) \). It can be expressed as

\[ G(s) = F(s)e^{-\tau_d s} = \frac{A_0 e^{-\tau_d s}}{(1 + \tau_1 s)(1 + \tau_2 s)} \]  \hspace{1cm} (11)

The closed-loop transfer function \( H(s) \) for Fig.5 is written as

\[ H(s) = \frac{V_o(s)}{V_{et}(s)} = \frac{1}{1 + G(s)} \]  \hspace{1cm} (12)

where \( V_{et}(s) \) is optimal control voltage and \( V_o(s) \) is the residual error. As \( t_d \) is introduced, it will cause instability if the loop parameters are not properly chosen. In order to make the loop work properly, it is better to limit the maximum delay \( t_{dmax} \)

\[ t_{dmax} \leq \frac{T}{5A_0} \]  \hspace{1cm} (13)

so that the loop is stable. Here, \( \tau = \sqrt{\tau_1^2 + \tau_2^2} \).

D. Accuracy of Pulse Width Control

The DC offset of the amplifier will influence the accuracy in pulse width control. Assume that when the two inputs of the amplifier are equal, the output level is denoted as \( V_{out0} \), and optimum control voltage is \( V_{et} \), then the DC offset \( V_{dco} \) is defined as

\[ V_{dco} = V_{out0} - V_{et} = A(V_o - V_{et}) = AE \]  \hspace{1cm} (14)

DC offset is unavoidable in practical design, and in a stable PWCL the offset is removed by creating an error \( E \) at the input of the amplifier. To reduce the error \( E \), a large gain in the amplifier is needed. However, on the other hand, when the gain of the amplifier increases, according to Eq.(13) \( C \) has to be increased to keep the loop stable. Increasing of \( C \) means more area, a compromise should be reached between the conflicting factors, area and performance.

IV. PWCL IMPLEMENTATION AND SIMULATION RESULTS

When the clock buffer has an even number of stages, the PWCL is configured as in Fig.6(a). The mechanism of the PWCL is: when the pulse width of \( V_o \) is wide it will make the pulse width on \( c+ \) wide too. So the N transistor have more time to discharge and \( V_c \) will drop, and then the output \( V_{et} \) will rise. As a consequence, the pulse width of \( V_o \) is narrowed. When the clock buffer is with an odd number of stages, the loop can be built as in Fig.6(b). CP1 is a charge pump to convert pulse width into current which charges or discharges the capacitor C. CP2 is another identical charge pump to create a reference bias voltage. When the input \( c- \) is connected to a clock with 50% duty cycle, the clock buffer output will also be adjusted to 50% if the loop is stable. When the incoming clock signal is not of 50% duty cycle, we can use a 3-inverter ring oscillator to create the reference clock signal as seen in Fig. 6(c). The difference between

II-543
Fig. 7. $f_c = 500\, MHz$, $A_0 = 50$, $C = 10\, pf$ and $t_r = t_f = 0.25T_s$, to create 50% duty cycle clock.

Fig. 8. $f_c = 333\, MHz$, $A_0 = 30$, $C = 10\, pf$ and $t_r = t_f = 0.25T_s$, to create 50% duty cycle clock.

$V_i$ and $V_{ref}$ is fed to the amplifier to generate the control voltage $V_{ref}$. This differential input reduces the difficulties in designing a perfect charge pump and bias circuit. Process dependence and temperature influence can be overcome as they appear in common mode.

A. Measurement

When the loop gain is properly chosen, $V_{ref}$ will finally converge as the Spice simulation on 0.6µm CMOS shown in Fig.7-8. Fig.7 depicts the response of a loop. The error $E$ is quite small so a good accuracy in pulse width is reached. If we double the N transistor size in the discharge branch, the transistor $M_a$ in Fig.4, of the charge pump CP1, we get the loop response and output clock as shown in Fig.8, where the clock duty cycle is about 33%.

In the measurement, the frequency of the input clock is 625MHz and through AC coupling and a bias circuit, we can adjust the input pulse width. The slope of the input signal is formed by an internal RC network. Curve 2 in Fig.9 shows the clock output of the buffer when the input signal, curve 1, has a duty cycle about 50%. Fig.9 also shows the case when the input signal duty cycle is about 50%.

REFERENCES


