

# COMPARISON OF STATIC LOGIC STYLES FOR LOW-VOLTAGE DIGITAL DESIGN

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## ABSTRACT

The most efficient approach in reducing dynamic power dissipation in digital circuits is to lower the supply voltage. This paper discusses gate-level power optimization through comparing static, non-clocked CMOS logic styles for low-voltage operation. Five promising logic styles were carefully analysed with a testbench to measure propagation delay and power dissipation as a function of supply voltage. The SCMOS logic style has good general characteristics. However, some logic styles, such as DCVSPG, DCVSL, and PPCL, proved to be quite promising in the low voltage region. This clearly suggests that a standard cell library designed for low-power could benefit of the mixed use of different logic styles.

## 1. INTRODUCTION

Power consumption has become one of the key issues in electronic systems. In order to address this problem efficiently, power consumption must be considered in all stages of the design flow. At the system level, various power-down modes reduce power consumption during idle periods. Algorithms can be modified for lower power in many applications. At the architectural level, increased parallelism and gated clocks can be used to reduce activity in digital circuits. Moreover, transistor sizing issues and process-related threshold voltage adjustment must be considered to achieve optimum power dissipation levels.

In CMOS circuits, total power dissipation is composed of static and dynamic components, where the dynamic part dominates in most semiconductor technologies. Dynamic power dissipation can be formulated as:

$$P_{dyn} = \alpha C_L V_{DD}^2 f$$

where  $\alpha$  is the activity factor of a system,  $C_L$  is the total load capacitance,  $V_{DD}$  is the supply voltage, and  $f$  is the clock rate. To simplify, the designer must reduce one or more of the previous factors to obtain a lower power dissipation figure for a system. Without trading off performance or speed, cutting down the clock rate can be achieved using parallel architectures and/or

pipelining with the expense of greater complexity and larger silicon area. The activity factor can be reduced by clever glitch-free circuits, but the cost is increased design time [1,2]. The load capacitance can be lowered by designing for the latest process technologies. Due to its quadratic dependence, system power consumption can be dramatically reduced by scaling down the supply voltage. However, the design trade-offs in this case are increasing propagation delays and decreasing noise margins.

In this paper, a number of static CMOS logic styles are investigated with respect of their usability in low-power designs. First, five prominent logic styles are illustrated and some key characteristics are shortly explained. A testbench for comparison of these logic styles is described and simulation results, in terms of propagation delay and power dissipation, are studied in detail. Finally, conclusions are drawn on the basis of these results.

## 2. LOGIC STYLES

A logic style is the way how a logic gate is constructed from a set of transistors. In this section, five static (i.e. non-clocked) CMOS logic styles are introduced.

### 2.1 Static CMOS

Static CMOS (SCMOS) is the most common of logic styles mainly because it is simple, robust, and easy to design. SCMOS is characterised by very good current driving capabilities and high noise margins. In Fig. 1a, a 2-input NAND gate is constructed using the SCMOS logic style.

### 2.2 Pseudo-NMOS

Pseudo-NMOS logic style has a similar NMOS pull-down network as SCMOS. As shown in Fig. 1b, the PMOS pull-up network is made of one PMOS transistor that has its gate connected to the ground. Hence, the PMOS transistor is continuously drawing current from the power supply which causes very undesirable static power dissipation when the NMOS tree is conducting. However, if a pseudo-NMOS gate is to produce logical ones most of the time, the static power dissipation can be minimised. Pseudo-NMOS logic style is ratioed

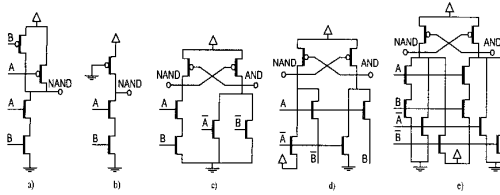


Figure 1. Logic styles: a) SCMOS and b) Pseudo-NMOS NAND gates, c) DCVSL, d) DCVSPG, and e) PPCL AND/NAND gates.

which means the output transition depends on the ratio of NMOS and PMOS transistor widths. The transistor count is less than that of SCMOS.

### 2.3 DCVSL

Differential Cascode Voltage Switch logic (DCVSL), depicted in Fig. 1c, comprises two parts: complementary NMOS pull-down networks and PMOS load transistors [3]. Logical function is formed solely using the NMOS transistors. The PMOS pull-up stage is needed to produce the correct logic levels to the outputs. The transistor configuration below the NAND node comprises two NMOS transistors in series as in the SCMOS NAND gate. The AND node is connected to a complementary function (NOR) of the complementary inputs. The DCVSL allows a logical function and its complement to be implemented by sharing parts of the NMOS trees, as in an XOR gate [4]. The logic depth of the DCVSL can be quite high, and reliability and noise immunity are very good. Dual rail wiring, high transistor count in some functions, and somewhat ratioed nature are the main drawbacks of this logic style [5].

### 2.4 DCVSPG

Differential Cascode Voltage Switch logic with Pass Gate (DCVSPG), see Fig. 1d, combines the best properties of the pass gate logic and DCVSL [6]. In pass gate logic, NMOS transistors are utilized as electronic valves which pass the desired logical values to the outputs. Both NMOS and PMOS transistors contribute to the pull-up of the output nodes. Therefore, the DCVSPG is immune to the floating node effect inherent in DCVSL.

### 2.5 PPCL

Push-Pull Cascode Logic (PPCL) is another logic style featuring a pull-up stage similar to the DCVSL [7]. A logical function is formed as in Fig. 1e. The NMOS transistors pass the desired value to the outputs directly from either the supply or the ground. This circuit structure reduces input capacitance and input driving requirements but the penalty is larger internal capacitance and body effect due to the increased transistor count.

## 2.6 Other Logic Styles

Several other logic styles were also studied, but their characteristics were not found suitable for low-voltage operation. The evaluated logic styles were: Cascode Non-Threshold Logic (CNTL) [8], Complementary Pass-gate Logic (CPL) [9], Double Pass-Transistor Logic (DPL) [10], Differential Pass-Transistor Logic (DPTL) [11], Energy Economized Pass-Transistor Logic (EEPL) [12], and single-ended pass-gate logic (LEAP) [13]. These logic styles either produced ambiguous logical values in the low-voltage ( $V_{DD} < 3*V_{Th}$ ) region or they had unacceptable propagation delays. These logic styles share some common features such as internal nodes within a logic gate and consequent buffered outputs. The inherent internal capacitances are particularly difficult to drive in the low-voltage region because of the reduced transistor drain current. Pass-transistor logic styles featuring only NMOS transistors can not deliver perfect logical ones, and thus, they require level-restoring output buffers. When the nominal supply voltage is employed, the level-restoring buffers operate properly, but in low voltages there is serious degradation in both functionality and speed.

## 3. SIMULATION

### 3.1 Setup

The circuit simulations were carried out using the device parameters of a 0.35 mm CMOS process technology that has a nominal supply voltage of 3.3 V. In the test circuits, the largest transistor width for PMOS was restricted to  $W_p = 1.8$  mm and all the NMOS transistors are minimal width devices,  $W_n = 0.6$  mm. The threshold voltages for NMOS and PMOS transistors are 0.52 V and -0.65 V, respectively. In all simulations, the HSPICE simulator was used for analysis.

### 3.2 Testbench

The testbench for comparing the different logic families was a chain of four full adders, as shown in Fig. 2b. Full adders were constructed from a set of basic logic gates which were implemented using the chosen logic styles. This allows comparison of the characteristics of the logic gates instead of full adder structures. An SCMOS full adder realized with four different logic gates is depicted in Fig. 2a. Thus, a full adder realizes the following logical equations:

$$C_{out} = AB + BC_i + AC_i$$

$$Sum = ABC_i + \overline{C_o}(A + B + C_i)$$

The full adder structure for the other logic styles had only minor variations in the differential logic styles

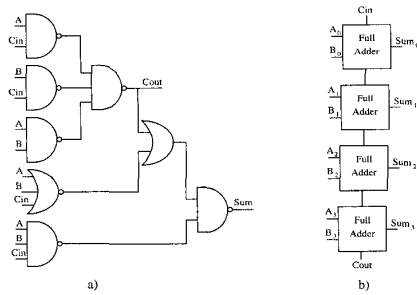


Figure 2. a) SCMOS full adder structure, b) testbench configuration.

(DCVSL, DCVSPG, PPCL) because of their complementary outputs. The transistor counts and widths for each full adder structure are summarized in Table 1. In simulations, one input was held high and the other inputs low and then the carry-in was triggered to the first adder to make it ripple to the carry-out of the fourth adder. Each output drove a 20 fF capacitive load.

full adder	nmos count	pmos count	total count	$\Sigma W_n$ $\mu\text{m}$	$\Sigma W_p$ $\mu\text{m}$	$\Sigma W_{n+p}$ $\mu\text{m}$
SCMOS	20	20	40	12.0	36.0	48.0
Pseudo-NMOS	20	9	29	123.0	5.4	17.4
DCVSL	38	16	54	22.8	14.4	37.2
DCVSPG	44	16	60	26.4	19.2	45.6
PPCL	76	16	92	45.6	38.4	84.0

Table 1. Transistor counts and widths for full adders

## 4. RESULTS

### 4.1 Propagation delay

Propagation delays are shown in Fig. 3. In the upper figure, absolute propagation delays from the simulations are shown. In the lower graph, the propagation delays are normalized to SCMOS. For the supply voltages above 1.0 V, pseudo-NMOS seems to be the fastest logic style, but it suffers from its continuously conducting PMOS load transistor which causes a slow high to low transition. It was impossible to design a minimum width Pseudo-NMOS gate with equal rise and fall times for even a small supply voltage range in this process technology. SCMOS, DCVSPG and PPCL have little distinction in terms of circuit speed.

A significant increase in propagation delays can be observed near 1.1-1.2 V that is the sum of the magnitudes of NMOS and PMOS threshold voltages. This area is generally known as the practical lower limit of logical gate operation. Lowering the supply voltage

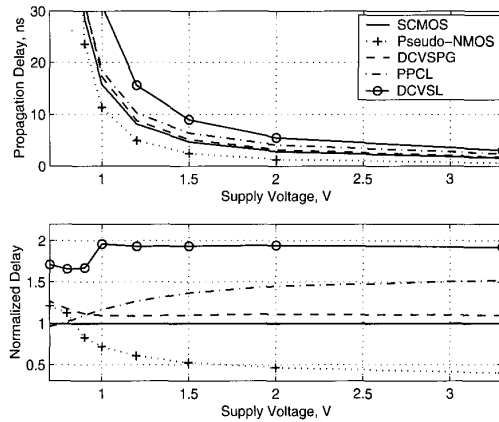


Figure 3. Upper: absolute propagation delays in the test bench. Lower: propagation delays normalized to SCMOS.

even further causes the transistors to operate in the weak inversion (subthreshold) region where process variations have fatal effects on logical gate functionality and speed. Furthermore, if the fan-in of a gate is increased, the internal capacitance and the body effect will increase causing also a serious slow-down in the operation. Due to the poor mobility of the charge carriers, a long chain of PMOS transistors in series was found particularly detrimental.

### 4.2 Power Dissipation

Fig. 4 shows the power dissipation of selected logic styles as a function of voltage. In the lower graph, power dissipation is normalized to SCMOS. Pseudo-NMOS suffers from static power dissipation and, consequently, is the most power-hungry logic style. DCVSPG, DCVSL, and SCMOS have the lowest power dissipation in these simulations. PPCL has a power consumption that is approximately double that of SCMOS.

Power-delay product (PDP) and power-delay<sup>2</sup> product (PDDP) values were calculated for each of the selected

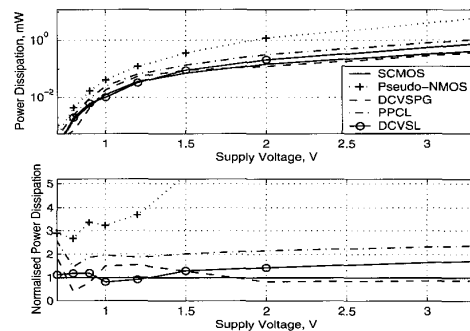


Figure 4. Upper: average power dissipation. Lower: average power dissipation normalized to SCMOS.

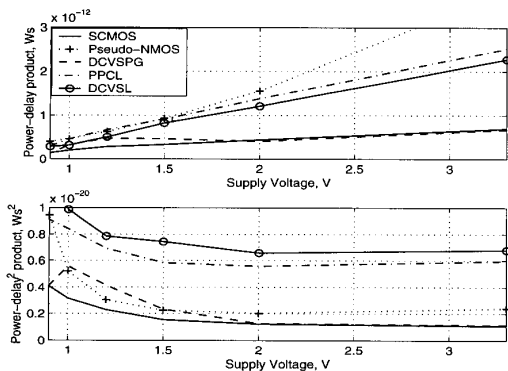


Figure 5. Upper: power-delay products. Lower: power-delay<sup>2</sup> products.

logic styles. The results are depicted in Fig. 5. The PDPs decrease gradually for all the logic styles as the supply voltage is lowered. PDDP puts more emphasis on circuit speed, and thus gives better guidelines for performance. The PDDPs remain nearly constant down to 1.5 V, below which they begin to increase rapidly. The SCMOS outperforms other logic styles almost in the entire voltage range.

## 5. CONCLUSIONS

Five logic styles were evaluated to compare their behaviour in the low-voltage region. The SCMOS had the best low-voltage speed and power dissipation characteristics in this study. However, a feasible approach is to design some individual low-voltage, low-power gates for standard cell libraries using DCVSPG, DCVSL, or PPCL that outperform the corresponding SCMOS gates. In the process technology utilized for this analysis, the attractive point for circuit operation lies near 1.5 V. In this voltage range, the propagation delay is approximately three times greater than with the nominal 3.3 V supply voltage, but the power dissipation is reduced by one order of magnitude.

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