

# Low Power CMOS Digital Circuit Design Methodologies with Reduced Voltage Swing

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## Abstract

In this paper, two techniques on low power circuit design, namely, Clock Separated Logic and Sub- $V_{dd}$  Voltage-swing Interfacing, are introduced. In the former method, reduced voltage-swing at internal nodes is used to achieve relatively low power dissipation as compared to circuits with full voltage-swing. In the latter method, pass-transistor logic with suppressed internal voltage-swing is used to reduce power dissipation on pass-transistor chain. Basic techniques on design of these circuits are investigated and analyzed.

## 1 Introduction

As clock rate of circuits and systems increases year by year, power consumption has become an important consideration in circuit design. Power reduction on process technology, architecture design, and circuit design had become more and more important for portable low power electronic equipments. CMOS had its largest market share in the last decade and in early 90's. However, there is serious increase in gate delay as operating voltage is reduced to 2V or less [1]. On the other hand, pass-transistor logics had become one of the most attractive logic families, from a view point of power consumption [2]. In addition, another new approach on combinational logic architecture had suggested the reduction of operating power by suppressing the signal swing to less than 1V[3]. As a result, pass-transistor logic is one of the most promising logic families on low power consumption.

Furthermore, internal signal propagation with voltage swing less than supply voltage have been proposed through various architecture or structures.

In concerning power consumption of circuits, dynamic power is considered to be main portion [4]. Equation of the estimation of the dynamic power is :

$$P_{dyn} = \sum_{i=1}^N c_i f_i V_{sw}(i) V_{dd} \dots \dots \dots (1)$$

where  $V_{sw}(i)$  is the voltage swing at node  $i$ ,  
 $c_i$  is the capacitance at node  $i$ , and  
 $f_i$  is the frequency of voltage switching at node  $i$ .  
The choice of  $V_{dd}$  is always considered to be  $V_{dd} = 3V_{tmin}$ .  
However, in pass-transistor logic, to account for the drop of one threshold voltage,  $V_t$ , in the transversal transistors, the choice of  $V_{dd}$  should be  $V_{dd} = 4V_{tmin}$ .

Reduction in supply voltage is one of the most important trend in low power digital design[5]. However, a decrease in the supply voltage will bring about various circuit design problems: drivability of MOST's will decrease, signals will become smaller, and the threshold voltage variation will be more limiting. One method in achieving power-off strategies is the introduction of the dual-rail coding, or the complementary coding logics, which is implicit in certain logic families such as the DCVSL[6]. However, the dual-rail DCVSL family consumes at least twice more in energy per input

transition than a conventional static family[7]. Another attractive logic family is the complementary pass-transistor logic (CPL)[8] [2].

The concept of hyper design domain is introduced in Fig. 1. In traditional digital design, voltage-swing and supply voltage are always kept constant. This design methodology will certainly lead to a limit in achieving low-power or high-speed design. However, if more than one voltage-swing value or transistor threshold voltage is chosen, new domain in design can be explored. In this paper, two of the emerging techniques based on the concept of hyper design domain, namely, Clock Separated Logic and Sub- $V_{dd}$  Voltage-swing Interfacing, are introduced.

## 2 Clock Separated Logic (CSL)

A Clock Separated Dynamic D-type flipflop (CSL-DFF) aims for low power logic circuit design is proposed [9]. The fan-in of clock signal, Ck, at the CSL-DFF is only connected to 4 transistors instead of 8 in complex-gate-DFF (Fig. 2). Low power consumption can be obtained by reducing voltage swing at both internal signal nodes and driving clock. Calculation and simulation result showed that a choice of aspect ratio of 10 on pMOS and 5 on nMOS would result in an average reduction of consumption power of about 50 percents using standard  $1.0\mu m$  gate length CMOS technology. The proposed circuit gives an average reduction of consumption power of about 30 percents as compared to complex-gate static D-type Flip-flop while giving a 20-percent of improvement on clock-to-output propagation delay[9]. According to analysis on the circuit of CSL-DFF, the longest propagation delay [9] is given by:

$$t_{pd}^+ = t_{pd}^- + t_r = a_1 + a_2 W_s + \frac{a_3 C_L}{W_s} \dots \dots \dots (2)$$

where  $W_s$  is the width of the pMOS transistors, and  $a_1, a_2, a_3$  are constants. It is noted that the minimum propagation delay can be obtained by adjusting  $W_s$  according to number of fan-out or loading.

### 2.1. Power Consumption

In concerning low power consumption, CMOS is always supposed to the best circuit configuration. However, since there is redundancy in most CMOS circuits, the parasitic capacitance would result in unintended power loss.

In CSL, however, parasitic capacitance is minimized without affecting the logic structure of the circuit. In addition, voltage in internal nodes is of  $sub - V_{dd}$  swing instead of full  $V_{dd}$  swing.

On the contrary, in domino or TSPC dynamic logics, there will be continuous charge/discharge in internal nodes such that power dissipation is relatively high [4]. For example, in the TSPC latch (or DFF) [10], charging and discharging occurs on every clock cycle even if the input data is not

changed (non-shuffle). It will result in unintended power loss due to the pre-charge operation.

## 2.2. Result

The power dissipation of the circuits on different clock frequency is illustrated in Fig. 3. Power dissipation was compared on four types of DFFs (single-rail True Single Phase Clock: TSPC [10], complex-gate static, dual-rail pass-transistor logic, and CSL). It is shown that CSL-DFF can achieve low power dissipation while attaining relatively high operating frequency. Simulation result showed that a choice of aspect ratio of 10 on pMOS and 5 on nMOS would result in an average reduction of consumption power of about 30 percents as compared to complex-gate static D-type Flip-flop while giving a 20-percent of improvement on clock-to-output propagation delay. Device parameters are based on standard  $1.0\mu m$  gate length CMOS technology, with transconductances  $K_n=150\mu A/V^2$ ,  $K_p=38\mu A/V^2$  and threshold voltages,  $V_{Tn}=0.5V$ ,  $V_{Tp}=-0.5V$ , where indices n and p represent nMOST and pMOST respectively.

In short, CSL is characterized by the isolation of current flow in half clock cycles. And, voltage swing in internal nodes is reduced by a threshold voltage drop at the cross-coupled transistor pair and clock signal can also be reduced to certain extent, according to application. However, disadvantages of this circuit are the necessity of complementary inputs and difference in Q and QB output propagation delays.

## 3 Reduced (Sub- $V_{dd}$ ) Voltage-swing Interfacing

Another low power circuit design methodology is the application of sub- $V_{dd}$  internal signals[3]. Consider the circuit connection in Fig. 4, which is applicable in both pass-transistor logic and CPL. The overall propagation delay includes (1) the delay on the inverter (or driver) that drives the transistor chain, (2) delay on the transistor chain, and (3) the receiver delay. The driver is an inverter with pMOST and nMOST of low threshold voltages, and scaled supply voltages ( $V_{cl}$  and  $V_{sl}$ ), while the receiver is an ordinary inverter with pMOST and nMOST of normal threshold voltages, and unscaled supply voltages ( $V_{dd}$  and 0). It is noted that delay on conventional scheme increases drastically as  $V_{dd}$  is less than 2V. However, the driver-receiver link with reduced logic signal swing can attain high performance even as the voltage swing is scaled down to about 0.6V. This result is consistent with the work of Nakagome [1].

In concerning the ratio of scaling of logic signal swing, calculation and simulation were done on the transistor chain. For preliminary analysis, the delay time on the fall time or rise time is estimated by

$$t_f = t_r = \frac{C_L}{\beta_n} \frac{2[V'_{tn} - 0.1(1 - 2\gamma)V_{dd}]}{[(1 - \gamma)V_{dd} - V'_{tn}]^2} + \frac{C_L}{\beta_n[(1 - \gamma)V_{dd} - V'_{tn}]} \ln \left[ \frac{(19 - 28\gamma)V_{dd} - 20V'_{tn}}{(1 + 8\gamma)V_{dd}} \right] \dots \dots \dots (3)$$

where  $\gamma$  is an index for scaling,  $V'_{tn}$  is the low valued nMOST threshold voltage,  $\beta_n$  is the conduction factor of nMOST, and  $C_L$  is the effective load capacitance.

It is in contrast to the delay in conventional inverter[4]:

$$t_f = t_r = \frac{C_L}{\beta_n} \frac{2(V_{tn} - 0.1V_{dd})}{(V_{dd} - V_{tn})^2} +$$

$$\frac{C_L}{\beta_n(V_{dd} - V_{tn})} \ln \left[ \frac{19V_{dd} - 20V_{tn}}{V_{dd}} \right] \dots \dots \dots (4)$$

where  $V_{tn}$  is the normal nMOST threshold voltage, It is estimated that a choice of  $\gamma$  on 0.10 to 0.20 is suitable in sub- $V_{dd}$  voltage-swing.

The total power consumption is estimated by:

$$P_{total} = P_d + P_s + P_o = P_d + P_s + I_o V_{dd} \dots \dots \dots (5)$$

where  $P_d$  is the dynamic power,  $P_s$  is the short-circuit power,  $P_o$  is the static power (power dissipation due to leakage current), and  $I_o$  is the leakage current.

The dynamic power consumption is defined in Eq. (1). The short-circuit current power consumption is given by

$$P_s = f_{clock} I_{mean} V_{dd} \dots \dots \dots (6)$$

And, the leakage current is defined by an exponential function on gate-source voltage[4].

Results on a bulk-MOSFET model suggested that normalized propagation delay and power dissipation of a driver-receiver link should be given by Table 1.

It is noted that with the introduction of low- $V_{th}$  transistor, propagation delay of a driver-receiver unit can be cut to about one-third as compared to that of inverter-inverter unit with high- $V_{th}$  transistors. In concerning power dissipation, the penalty will happen in leakage current and short-circuit current. However, in compared with the dominant portion of the dynamic power, these factors has become negligible. On the other hand, as concerning circuit design on low supply voltage and exclusive low- $V_{th}$  transistors, power dissipation can be kept small (1/3) while achieving medium operating speed. As a result, design methodology depends mainly on a trade-off between expected operating speed and available fabrication technology.

One of the criteria to minimize dynamic power can be reflected by the Dynamic Power Factor:

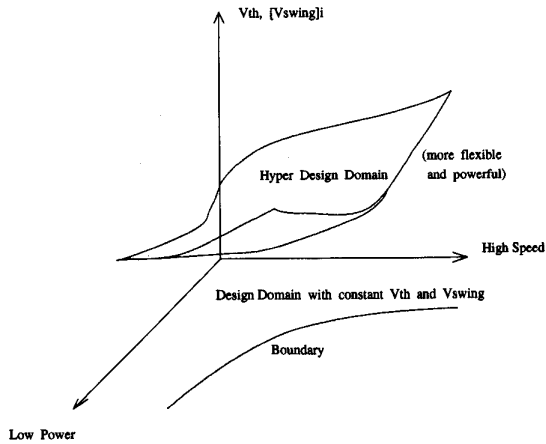
$$DPF = \sum_{i=1}^N c_i V_{sw}(i) \dots \dots \dots (7)$$

With reduced voltage-swing, it is noted that dynamic power can be reduced (Fig. 5).

## 4 Discussion

In general, the key to low power high speed logic design is a proper choice of supply voltage and threshold voltage. On a measurement on high frequency operation of an inverter array with transistor threshold voltages,  $V_{Tn}=0.3V$ ,  $V_{Tp}=-0.3V$ , leakage current is of the order of 40nA at  $V_{dd}=2.0V$  [11]. It reflects the corresponding value of static power in the power-off mode of CSL. Although this value convinces a higher static power than prediction in modeling (Table 1), the value is negligible as compared to dynamic power or short-circuit power. In the application of sub- $V_{dd}$  voltage-swing, Multiple-valued-Threshold CMOS (MTCMOS) is one of the solutions[12]. Practical data on temperature sensitivity suggests that MTCMOS can perform better than (more stable) conventional CMOS. For instance, the average temperature coefficient of propagation delay of logic gates on MTCMOS can be reduced to 0.10%/degree below 80C, while that of conventional CMOS is 0.14%.

Upon several investigation on CSL and sub- $V_{dd}$  voltage-swing interfacing logics, low power digital design can be



Examples on Hyper-Design Domain:

- (1) Reduced Swing in Data Line
- (2) Reduced Swing in Clock Signals (CSL)
- (3) Sub-V<sub>dd</sub> Interfacing
- (4) Reduced Swing CSL

Figure 1: Concept of the hyper design domain

achieved without loss of stability and reliability on these two design methods.

A comparison on the performance of CMOS, CSL, CPL, Sub-V<sub>dd</sub> CPL, and dynamic logic are given in Table 2. It is noted that features on different logic techniques are various. The choice and tradeoff of technology depend mainly on application and speed-power requirement.

Further application of reduced voltage-swing techniques can be found in [13], in which reduced signal swing on data bus is achieved by termination resistors. DPF on such architecture is very low because magnitude of the signal is suppressed to less than one-tenth of the supply voltage. Another type of low swing circuit scheme was developed by [14] in which half-swing clock signal is used to reduce power consumption on clock circuitry. In this method, a practical reduction of 67 percents of power was established on a latch circuit, while the theoretical limit is a reduction of 75 percents at the clock drive.

## 5 Conclusion

Several methodologies in low power digital design are discussed and two of the new circuit design techniques are proposed: CSL and Sub-V<sub>dd</sub> Voltage-swing Interfacing. In CSL, power dissipation is reduced with the reduced number of transistors and with the introduction of the clock separation transistors on vertical transistor tree. In the Sub-V<sub>dd</sub> Voltage-swing Interfacing technique, multiple voltage supplies are used to drive internal signal levels. High speed transition is achieved by MTCMOS. However, there is still difficulty in the fabrication process. In addition, further reduction in voltages at internal nodes can reduce the power dissipation to certain extent, in accordance with application.

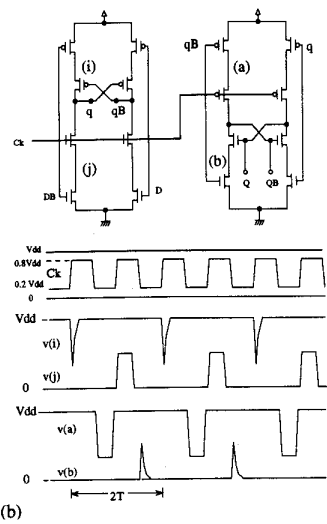
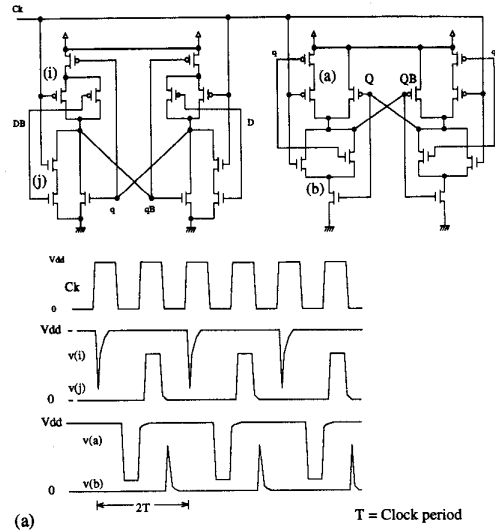


Figure 2: Internal voltage-swing in (a) complex-gate DFF, and (b) CSL-DFF

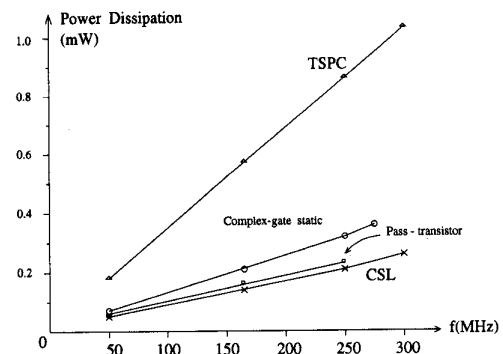


Figure 3: Power dissipation of different circuit configurations versus operating frequency

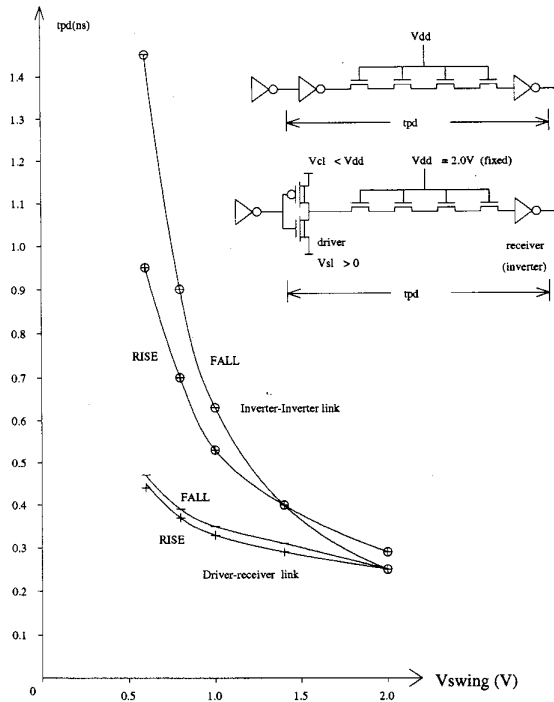


Figure 4: Simulated propagation delay versus logic signal swing

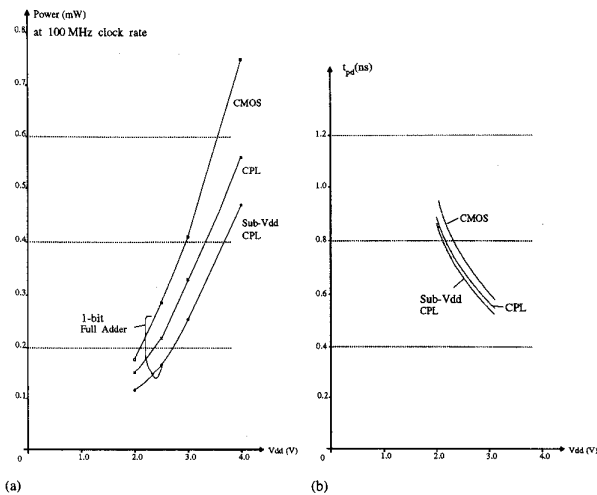


Figure 5: Comparison of features of CMOS, CPL and sub-Vdd CPL full adder: (a) power consumption, and (b) propagation delay.

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Table 1. Comparison of normalized delay and power dissipation on full swing and reduced swing logics

	Reduced Swing Low Vth	Full V <sub>dd</sub> swing High Vth
Normalized delay	7.92	27
Leak current	4.8pA	2.4pA
Short-circuit power	0.201mW	0.125mW
Dynamic power (at 250MHz)	16mW	16mW

Table 2. Comparison of performance of different logic circuit techniques

	CMOS	CSL	CPL
Power dissipation	Medium	Low	Low
Speed	Medium	Fast	Fast
Stability (Noise margin)	Excellent	Good	Good
Stability (Power-off mode)	Excellent	Medium	Medium
Immunity to noise from clock signal	Strong	Medium	Weak

	sub-V <sub>dd</sub> CPL	TSPC
Power dissipation	Lower	High
Speed	Fast	Very Fast
Stability (Noise margin)	Good	Medium
Stability (Power-off mode)	Medium	Bad
Immunity to noise from clock signal	Weak	Weak