

Fast CMOS ECL Receivers With 100-mV Worst-Case Sensitivity

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Abstract—CMOS ECL receiver circuits consisting of a differential amplifier stage and a CMOS inverter are shown to convert 100-mV input signals to on-chip CMOS levels even with worst-case parameter variations in a 5-V 1- μ m technology. The same ECL receivers in submicrometer CMOS technology have higher speeds and better sensitivity, with smaller worst-case-to-best-case variations. Two different receiver circuits are used to cover a range of power supply options; a third circuit provides a comparison case. The differential amplifiers feature built-in feedback compensation for common-mode parameter variations. The differential input devices are designed with large widths, minimum channel lengths, and an interleaved layout to enhance gain, speed, and margin for differential mismatches. The simplicity of the circuits and the effectiveness of the built-in compensation facilitate analysis. Partitioning and simplifying assumptions are used to thoroughly test the worst case without complex simulations, while providing insight into the design process. Simulated and measured results demonstrate feasibility for 100-mV worst-case sensitivity for CMOS ECL receivers in 1- μ m technology, with no substantial access-time penalty in going from TTL to ECL interfaces.

I. INTRODUCTION

CMOS AMPLIFIERS in 5-V 1- μ m CMOS technology can serve as asynchronous receivers of high-speed ECL signals with 100-mV worst-case sensitivity. As the technology is scaled to submicrometer dimensions with reduced power supply voltages, these same receivers have even higher speed and better sensitivity. CMOS ECL receivers are needed for the small-signal interfaces required to use CMOS SRAM and logic in high-speed systems to the best advantage.

CMOS SRAM's are offering increasingly high-speed access times in addition to the well-known CMOS features of low power, robust operation, scalability, high density, and yield. Aggressive progress in MOS SRAM access time at the 64K level is evident from the Fig. 1 plot of access times versus year reported (see [1]–[5] for examples of the faster SRAM's referenced in the figure). The trend line is every bit as steep at the 256K level and no doubt will

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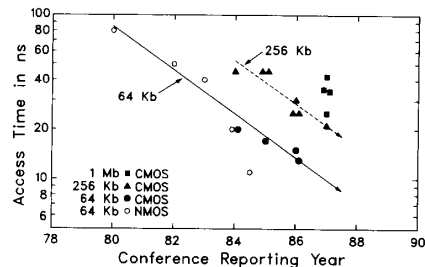


Fig. 1. Progress in SRAM access time. Plot of access time as reported at conferences ([1]–[5]) for NMOS and CMOS SRAM with TTL interfaces. In the projected sub-10-ns access-time regime, chip-to-chip crossing delays could exceed on-chip delays if TTL interfaces continue to be used.

continue at 1 Mbit. With RAM's in the sub-10-ns regime, however, use of TTL interfaces and networks can easily result in chip-to-chip crossing delays exceeding on-chip delays.

Reduction of chip-to-chip crossing delays in large systems through use of small-signal transmission-line networks is a well-established art in the ECL bipolar world [6]. High-speed CMOS SRAM and logic can realize similar advantages if CMOS can be retrofit to a bipolar ECL environment or if conventional ECL standards can be adapted for use in all CMOS systems or modules. Either case involves designing CMOS off-chip drivers and termination schemes, among other wide-ranging issues. However, the design of asynchronous CMOS ECL receivers having better than 100-mV worst-case sensitivity without adding substantially to the access time is one of the more difficult parts of the problem.

The CMOS ECL receivers analyzed in this paper simply consist of a single differential amplifier stage with built-in compensation, followed by a CMOS inverter. Previously reported CMOS ECL receivers have used a much larger number of devices and complex bias and compensation schemes [7], [8]. The more complex circuitry is more susceptible to mismatches in devices, power distribution, and noise. Additionally, the analysis becomes substantially more complicated as the number of devices grows and as they are distributed more widely in the physical layout of the chip. The analysis shown in this paper indicates that

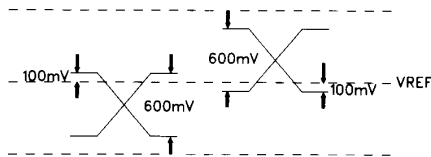


Fig. 2. Worst-case approximation of signal levels at receiver input. Worst-case single-rail amplitude relative to the reference is assumed to be 100 mV. Dual-rail signals with correlated common-mode shift could provide a 600-mV signal amplitude.

this complexity is not required to meet a 100-mV worst-case sensitivity specification.

The analysis shown uses simplifying assumptions and partitioning to allow a thorough testing of the receiver circuits without requiring complex simulation. The analysis techniques previously given for CMOS differential amplifiers [9] have focused on small-signal amplification for analog applications. A worst-case analysis has not been described for differential amplifiers as small-signal-to-large-signal converters with the large parameter variations that are typical in digital CMOS.

The signal level and power supply assumptions are discussed first. Then three CMOS receiver circuits are described followed by an analysis of their sensitivity as limited by parameter variations and by an analysis of their speed as a function of input signal amplitude.

II. ECL INPUT SIGNALS AND POWER SUPPLY OPTIONS

What makes the receiver design difficult is the very small net signal available at the inputs. This signal in a high-speed large-machine environment is complicated to simulate in detail. All of the worst-case examples in this paper are simulated using the simplified representation of the input signal shown in Fig. 2. A single-ended signal relative to a reference voltage is assumed, with a net signal amplitude at the receiver input of 100 mV. This net amplitude is after losses due to noise, power supply, and reference voltage inaccuracies in the circuitry and transmission network external to the receiver.

The 100-mV worst-case amplitude is simulated as being steady state in this simplified representation. In most applications, the 100-mV minimum amplitude actually will increase as the noise generated by this signal and by coupling from other simultaneously switching signals decreases. As shown in Fig. 2, the time for switching from a maximum of 500-mV amplitude drive in the opposite direction is also included in the delay simulations.

Only single-ended input signals are assumed in this paper. Noted on Fig. 2, however, is the improvement in amplitude possible if dual-rail signals with correlated common-mode shift are available.

Where the reference voltage lies relative to the on-chip power supplies is key to receiver design. There is a wide variety of options to consider, depending on whether an established ECL bipolar standard must be retrofit or whether a more optimum set of supplies is available. A proposed 5-V CMOS system with a dedicated set of sup-

TABLE I
SOME POWER SUPPLY OPTIONS FOR SMALL-SIGNAL INTERFACES

	5V CMOS		Vendor 100K ECL	IBM ECL and <1 μ m CMOS
	Case I	Case II		
VDD	4.3V	2.5V	0V	1.4V
VREF	0V	0V	-1.3V	0V
VSS	-0.7V	-2.5V	-4.5V	-2.2V

plies and two different bipolar ECL systems (IBM and 100K) are considered as applications for the circuits described. To demonstrate feasibility for these applications in 5-V 1- μ m CMOS, subsequent sections of the paper show circuits and sensitivity analysis for the two cases given in Table I.

Case I, Table I, is aimed at applications wherein the supplies can be optimized for CMOS. It uses the IBM ECL convention of placing the reference at ground. However, the reference is set close to the most negative supply, chip ground, V_{SS} . This choice facilitates design of the off-chip driver. V_{SS} can define the signal down level; if a third power supply plane is available (at +0.7 V), it can define the signal up level. With this power supply set, no large on-chip voltage drops from V_{DD} or V_{SS} are required to set the off-chip driver signal levels. Additionally, enough overdrive is available for an all-NMOS off-chip driver. Since three power supply planes are used in this proposed CMOS system as well as in IBM ECL systems, similar package design and noise analysis [6] can be used.

Case II, Table I, places the reference voltage midway between V_{DD} and V_{SS} . This is a natural option to also consider for an all-CMOS system or module. More importantly, it can demonstrate feasibility for retrofitting bipolar ECL levels. The receiver circuit design shown for Case II in a 5-V 1- μ m CMOS technology can be 100K ECL compatible with an adjustment in device sizes to correct for the reference level being above the median V_{DD}/V_{SS} voltage, as is shown in the analysis section.

IBM ECL supplies place the reference closer to the median. However, the maximum power supply amplitude is only 3.6 V, which is more suitable for submicrometer technologies. As will be discussed later in the paper, the preferred Case II circuit in a 3.6-V scaled technology will have even better sensitivity than indicated by the 5-V 1- μ m analysis shown in this paper. This 3.6-V scaled version of the receiver is fully compatible with IBM ECL levels.

III. CMOS ECL RECEIVER CIRCUITS

A small number of analog stages is key to achieving both high speed and tight tolerances in CMOS. The three receiver circuits shown consist of a single differential-amplifier stage followed by a standard CMOS inverter. The differential amplifiers feature built-in compensation to common-mode shifts caused by parameter variations. Also featured are large width input devices to enhance gain and to minimize sensitivity to differential mismatches in devices. As a result of these features, minimum channel-length

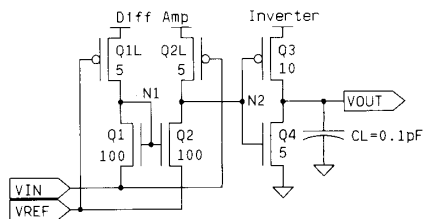


Fig. 3. DD CMOS ECL receiver.

design on critical devices can be used to maximize speed while still meeting the 100-mV worst-case specification.

The differential amplifier provides enough gain so that the second stage can be a standard CMOS inverter. The CMOS-inverter second stage provides some compensation relative to the differential amplifier for common-mode shifts in power supply and P-relative-to-N device parameters. As the analysis results show, on-chip CMOS levels are available at the inverter output under worst-case conditions. Consequently, after this point, standard or custom digital CMOS circuits can be used to develop more gain and for logic functions.

A preferred circuit is shown for each of the power supply cases; a third circuit is included for comparison. As is shown in the sensitivity analysis section, the preferred amplifiers both have good built-in compensation for parameter variations, whereas the compensation in the third circuit is inadequate for sensing of 100-mV input signals when parameter variations are worst case. Nominal power dissipation and transient delay in all three circuits are nearly identical.

A. Direct-Drive CMOS ECL Receiver

The direct-drive (DD) receiver circuit is shown in Fig. 3. The differential-amplifier input stage is designed for Case I supplies wherein the reference level is near chip ground. The signal is supplied directly to the sources of the differential N-channel input devices Q_1 and Q_2 . The current sink requirement of the inputs is limited by P-channel load devices Q_{1L} and Q_{2L} . With the device sizes shown, the current sinking requirement (0.5 mA) is tolerable for most applications in a terminated network with a small fan-out. Moreover, the current into the signal pin is constant enough to cause negligible signal attenuation.

The input signal is applied to the source of the diode-connected device Q_1 . It appears at N_1 , slightly amplified and level shifted up to give good overdrive to Q_2 . The inverted signal appears at the differential-amplifier output N_2 , amplified enough to drive the inverter output V_{OUT} to on-chip levels even under worst-case conditions.

Due to the biasing of Q_2 from the diode-connected Q_1 device and the direct drive of the P-channel load devices, the DD differential amplifier has very good tolerance to common-mode shifts in power supplies and P-relative-to-N device strength. For example, if the P devices become more conductive relative to the N devices, N_2 will tend to rise. However, N_1 will also rise, supplying a larger overdrive to

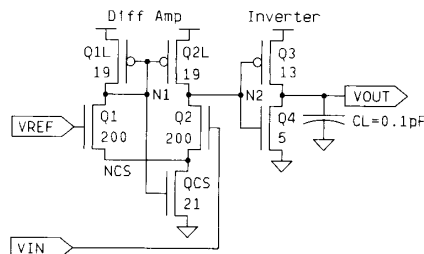


Fig. 4. DMC CMOS ECL receiver.

Q_2 , thereby pulling N_2 back down towards the design value. In addition, the P-load device gates are driven directly by the inputs with good overdrive, further enhancing the amplifier gain and minimizing sensitivity to threshold variations. The direct drive of the P devices permits use of larger than minimum channel-length devices to enhance output impedance without a significant speed penalty. The result is high speed and good tolerances for the DD receiver in applications wherein the reference voltage can be set near chip ground, such as in an all-CMOS high-speed system.

B. Double-Mirror-Compensated CMOS ECL Receiver

The double-mirror-compensated (DMC) CMOS receiver circuit (Fig. 4) is designed for a midrange reference voltage. The reference voltage and the input signal are supplied to the gates of the N-channel differential input devices Q_1 and Q_2 . The P-channel load devices Q_{1L} and Q_{2L} form the commonly used mirror bias configuration, with Q_{1L} being the diode-connected device. Not so usual is the biasing of the current-source device Q_{CS} from the mirror node N_1 . The signal appearing at N_1 is the input signal, slightly attenuated. It drives both the load device Q_{2L} and the current-source device Q_{CS} in the direction to enhance the gain at the output of the differential amplifier. As with the DD circuit, the gain at the differential-amplifier output is enough to drive the inverter output to on-chip CMOS levels even under worst-case conditions.

The double-feedback biasing of both Q_{2L} and Q_{CS} from the mirror node N_1 provides very good compensation for power supply and P-relative-to-N device common-mode shifts, similar to that seen in the DD amplifier. Moreover, the shift in N_2 with these types of variations matches very well those in the inverter, resulting in very little offset at the inverter output. The ratio between Q_{2L} and Q_{CS} determines the biasing of N_2 , since the differential input devices are so large. With Q_{2L} and Q_{CS} being both driven from the same node, they look very much like an inverter in their response to variations in thresholds and power supplies.

C. Standard CMOS ECL Receiver

The more standard (SD) differential amplifier (Fig. 5) serves as a comparison case. It uses mirror-connected P devices, but the current-source gate is simply connected to

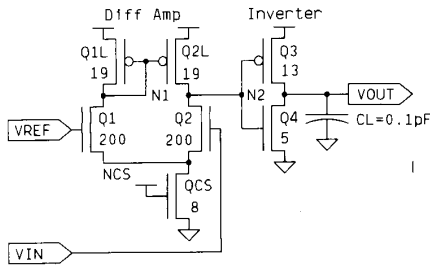


Fig. 5. SD CMOS ECL receiver.

V_{DD} . The Q_{CS} device width has been adjusted so that the standing current is equal to that for the DMC amplifier. Under nominal conditions, the SD circuit performance is very similar to that found with the DMC circuit. Under worst-case conditions, however, the poor compensation in the current-source biasing results in too large of an offset for sensing of 100-mV input signal amplitudes (see Section IV).

We explored many different ways to bias the current source other than those shown here, but none improve on the performance of the simple biasing used in the DMC circuit. Substantial improvement over the SD circuit requires extra bias stages, resulting in higher power and larger susceptibility to mismatches in devices, noise, and power distribution. Therefore, the SD circuit provides the most straightforward comparison to illustrate the importance of built-in compensation for worst-case common-mode parameter variations.

IV. ANALYSIS OF SENSITIVITY AS A FUNCTION OF PARAMETER VARIATIONS

To simulate the sensitivity of the receiver circuits, the parameter variations, as outlined in Table II, are separated into two types: common mode and differential. Common-mode device variations shift all P devices together and all N devices together, whereas differential variations are mismatches between devices of the same type. The common-mode parameter variations can cause gain loss and have a nonlinear effect on input offset voltage, whereas differential variations have a much more linear effect on input offset voltage. In both cases (as with the simplified representation of the input signal), noise is considered as a steady-state loss of overdrive or as part of the threshold variation allotment.

Both the common-mode and the differential parameter variation categories are subdivided. In the common-mode case, the P-to-N threshold and conductances, power supply, and common-mode noise are simulated together. The temperature and common-mode input signal shift are simulated separately, because these are more application specific. In the case of differential variations, it is useful in the design process to consider the threshold and conductance mismatches separately, for reasons discussed later.

In all cases, the simulations were done using a comprehensive CMOS model matched to production hardware.

TABLE II
PARAMETER VARIATIONS

• Common-mode
→ P To N Threshold and Conductance
→ Power Supply and Common-mode Noise
→ Temperature
→ Common-mode Input Signal Shift
• Differential
→ Threshold Mismatch and Differential Noise
→ Conductance Mismatch

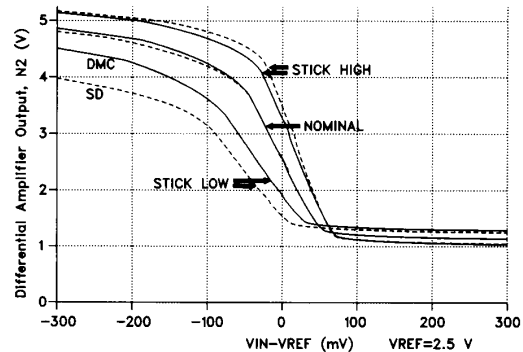


Fig. 6. Simulated transfer characteristics at differential-amplifier output for nominal and common-mode parameter variation cases. Worst-case common-mode parameter variations from Table III are applied to all devices in the direction to stick the differential-amplifier output N_2 high or low. The solid line is for the DMC receiver; the dashed line is for the SD receiver. The differential-amplifier output node N_2 is plotted as a function of the input scanning ± 300 mV relative to the reference (2.5 V).

Threshold and conductance variations are applied to all devices in the worst-case pattern. Measurements on CMOS ECL receivers from one run in a 1- μ m technology [10] are shown to indicate the validity of the conclusions drawn from the simulations. The measured case is worse than nominal but not as severe as the simulated worst case. First, simulated and measured results for common-mode device and power supply variations are described. Then, the effect of differential mismatches is discussed. Next, a simulation result with a worst-case set of both common-mode and differential variations at temperature is shown, followed by measured and simulated results with 100K ECL supplies.

A. Common-Mode Parameter Variations

Simulated transfer characteristics with power supply variations and with P-to-N threshold and conductance variations are plotted in Fig. 6. The nominal transfer characteristic for the DMC (solid line) and the SD differential amplifier (dashed line) are roughly equivalent. However, the worst-case common-mode parameter variations applied to all devices in the amplifiers results in a much larger offset voltage with the SD circuit. Table III lists the worst-case set of parameter variations used in this and the other simulations which will be shown.

Applying all the variations in the direction to stick the differential-amplifier output node low is the worst case for

TABLE III
SIMULATION RESULTS

PARAMETER SET TYPE	EXAMPLE WC VARIATIONS	DD RECEIVER Vos/GAIN	DMC RECEIVER Vos/GAIN	SD RECEIVER Vos/GAIN
Common-mode	$\Delta V_{DD} = \Delta V_{SS} = \pm 0.25V$ $\Delta L_{EFF} = 0.3\mu m$ $\Delta V_T = 0.4V$	11mV/28	3mV/18	27mV/13
Differential	$\Delta V_T = 30mV$ $\Delta g_m = 3\%$	24mV/37	34mV/27	34mV/26
Net Signal	100mV - total Vos	55mV	53mV	29mV

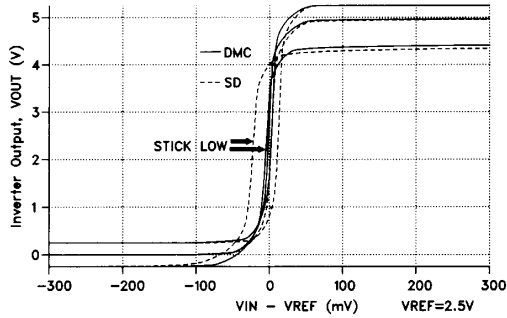


Fig. 7. Simulated transfer characteristics at the inverter output node for nominal and common-mode parameter variation cases. Worst-case common-mode parameter variations from Table III are applied to all devices in the direction to stick the differential-amplifier output N_2 high or low. The solid line is for the DMC receiver; the dashed line is for the SD receiver. The inverter output node N_2 is plotted as a function of the input scanning ± 300 mV relative to the reference (2.5 V).

both amplifiers. The input offset voltage for the stick-low and stick-high cases could be balanced by making the input devices (Q_1 and Q_2) smaller, but the input offset voltage due to differential mismatches would be increased. In the DD circuit, the input offset voltage is similar to that shown for the DMC circuit. However, because of the smaller input devices and the lack of connection to V_{SS} , applying the variations to stick the differential-amplifier output node high is the worst case.

Fig. 7 is a similar plot for the same cases as Fig. 6, but looking at the inverter output as a function of the receiver input signal. Virtually all of the offset in the DMC case is compensated by the inverter. The excess offset with the SD circuit is uncompensated by the inverter since it is due to the uncompensated biasing of the SD differential-amplifier current-source device.

Another way to test the margin in the amplifiers is shown by Figs. 8–10. These are plots of the linear region gain of the three differential amplifiers as the inputs are both scanned ± 1 V from the design value. Besides showing the impact of common-mode input voltage variations, this type of plot is a sensitive indicator of the margin remaining for common-mode parameter variations. Under nominal conditions, the DMC and SD circuits are similar, as shown in the Fig. 8 simulation results. However, with the worst-case set of common-mode parameter variations listed in Table III, the simulation results in Fig. 9 demonstrate the lack of margin in the SD case relative to the DMC case.

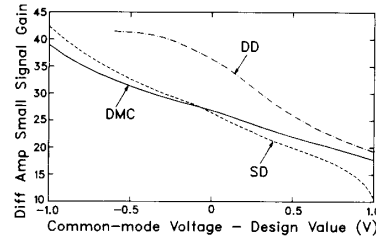


Fig. 8. Simulated nominal gain dynamic range. The nominal small-signal gain of the differential-amplifier stage is plotted as a function of the signal input and the reference input both being scanned ± 1 V from the design value.

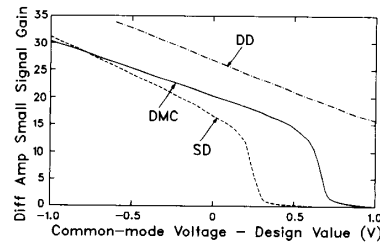


Fig. 9. Simulated worst-case gain dynamic range. The worst-case small-signal gain of the differential-amplifier stage is plotted as a function of the signal input and the reference input both being scanned ± 1 V from the design value. Common-mode parameter variations from Table III are applied to all devices in the worst-case pattern.

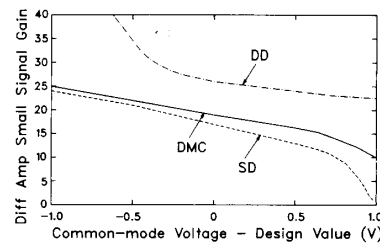


Fig. 10. Measured gain dynamic range. The measured small-signal gain of the differential-amplifier stage for each of the three receivers from the same chip is plotted as a function of the signal input and the reference input both being scanned ± 1 V from the design value. Measured parameter variations are given in Table IV.

Also evident from Figs. 8–10 are the high gain and the wide dynamic range available with the DD differential amplifier. In the application being considered, the range is limited by V_{SS} (the minimum signal down level) at the lower end. At the higher end, the range is limited by the input window required for the inverter second stage to have adequate noise margin.

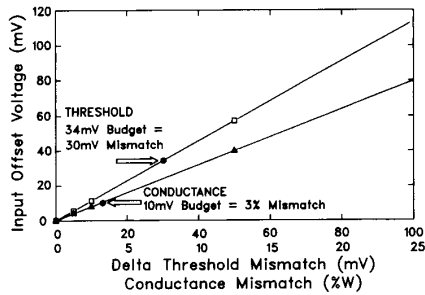


Fig. 11. Simulated impact of differential mismatches on input offset voltage in the DMC receiver. Mismatches between devices of the same type are applied to all devices in the worst-case pattern. Conductance mismatches are modeled as a percentage change in channel width.

Fig. 10 plots the dynamic range found from measured data on the three amplifiers from one typical chip. As listed in Table IV, this run happened to have a large shift in P-to-N device strength relative to the design value, while having small differential mismatches. Consequently, the measured gain and dynamic range is between the nominal and the worst-case example. The measured relative dynamic gain range of the amplifiers matches the predictions from the simulations reasonably well.

B. Differential Mismatches

The impact of differential mismatches on input offset voltages can be seen in the plot of Fig. 11 for the DMC circuit. A similar linear plot results from simulations of the DD and SD circuit, with input offset voltages as given in Table III. The input offset voltage was calculated from simulated transfer characteristics similar to Fig. 6, but with common-mode parameters being nominal and differential threshold and conductance mismatches being separately varied. Conductance mismatches were modeled as a percentage change in channel width to put the mismatch in terms which can be immediately related to design values. In either case, the differential mismatches are between devices of the same type, applied to all devices in the worst-case pattern.

Separately considering the threshold and conductance mismatches is useful to the design process. A major contributor to differential mismatches is local variations in the channel length of the short-channel devices used in the amplifiers for speed. For a given short-channel effect, the trade-off between input offset voltage and the channel-length design value can be investigated more readily by separating threshold and conductance effects. Additionally, an allotment for end-of-life shifts in threshold can be evaluated more easily. As indicated on Fig. 11 and Table III, for the worst-case example, we budgeted 34-mV input offset voltage for 30-mV threshold mismatch and 10-mV input offset voltage for 3-percent conductance mismatch. We have not found it necessary to use a larger than minimum channel-length design on the input devices to meet these specifications.

The impact of differential mismatches can be contained by using large input devices with careful physical design.

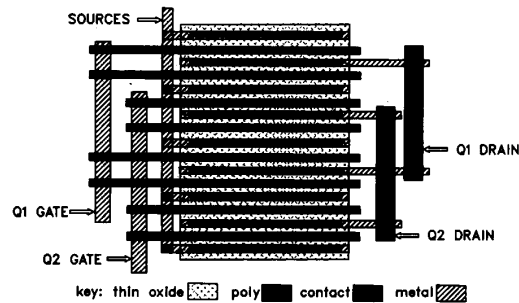


Fig. 12. Interleaved layout of interdigitated differential input devices.

The use of large width input devices maximizes gain and averaging of local variations in channel length. An example of an interleaved layout of interdigitated differential input devices Q_1 and Q_2 of the DMC circuit is shown in Fig. 12. The four poly fingers forming the gate of Q_1 are interleaved with the four fingers forming Q_2 , thereby providing better averaging of local variations. The drain contacts for each transistor are shared between gate fingers to minimize parasitic capacitances. The source contacts are wired in common.

Differential mismatches to be expected at end of life in the differential amplifiers are substantially less than need be specified for digital CMOS inverters and latches. A major contributor to end-of-life threshold shift is hot-electron injection into the gate oxide of the N devices. Relative to an inverter, the differential input devices have at least 1 V less voltage from gate to substrate to drive the hot-electron effect. Moreover, the current density in these large input devices is an order of magnitude lower, commensurately reducing the flux available for hot-electron injection.

C. Total Input Offset Voltage and Net Signal

Table III lists the input offset voltage V_{os} components for the worst-case example. The compensation built into the DMC and the DD circuits allows a small input offset-voltage budget for a fairly large allotment in common-mode parameter variations. The DD receiver has a higher input offset voltage than the DMC receiver with the same common-mode parameter variations, because it does not match the CMOS-inverter second stage quite as well as does the DMC circuit. In the case of the SD circuit, the lack of compensation for the current source results in substantially higher input offset voltage than seen with either the DMC or the DD receivers.

Differential mismatches account for most of the input offset voltage budget. The better drive to the P devices and the higher gain in the DD circuit results in a smaller sensitivity to threshold mismatches relative to the DMC and SD receivers.

When the total of input offset voltage components is subtracted from the assumed worst-case signal, the net signal for driving the receiver is more than 50 mV for both the DD and DMC receivers. This net signal times the

TABLE IV
MEASURED RESULTS

PARAMETER SET TYPE	EXAMPLE WC VARIATIONS	DD RECEIVER $V_{os}/GAIN$	DMC RECEIVER $V_{os}/GAIN$	SD RECEIVER $V_{os}/GAIN$
Common-mode	$\Delta VDD = \Delta VSS = 0.0V$ $\Delta LEFF = 0.3\mu m$ $\Delta VT = 0.08V$	2mV/30	2mV/25	4mV/20
Differential		3mV	6mV	6mV

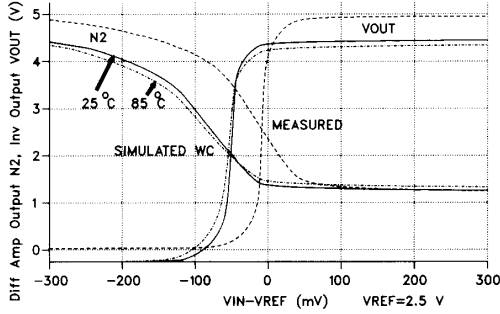


Fig. 13. DMC receiver transfer characteristics at the differential-amplifier output and the inverter output. The worst-case common-mode and differential parameters from Table III are applied to all devices in the worst-case pattern for the solid line simulation at 25°C and the dash-dot line simulation at 85°C. The dashed line plots the measured characteristics of a typical receiver from a run with the parameter variations as given in Table IV.

worst-case differential-amplifier gain results in enough swing at the differential-amplifier output to drive the inverter to on-chip CMOS levels for both the DD and DMC receivers. This is not the case for the SD receiver.

Measured input offset voltages and differential-amplifier gains are shown in Table IV. Measured transfer characteristics of V_{IN} versus N_1 , N_2 , and V_{OUT} were used to determine how much of the input offset voltage is due to common-mode parameter shifts and how much is due to differential mismatches. Common-mode parameter variations result in a shift of both N_1 and N_2 from the design value. Differential parameter variations result in a shift of N_1 relative to N_2 . As is noted in Table IV, a small common-mode input offset voltage was measured despite the fairly large shift in P-to-N device strength found in this run.

The set of transfer characteristics plotted in Fig. 13 illustrate the results shown in the tables. The measured transfer characteristics are plotted with the dashed line for a typical DMC receiver from the run characterized in Table IV. The simulated worst-case example is plotted with the solid line for room temperature and the dash-dot line for 85°C. This worst-case example includes both the common-mode and the differential parameter variations listed in Table III applied in the worst-case pattern to all devices. At ± 100 -mV input signal, on-chip CMOS levels are available at the inverter output.

The parameter control required by the worst-case example for both the DMC and DD circuit is well within the bounds of typical CMOS 1- μm processes. In a submicrometer process, the smaller magnitude of parameter variations and the higher gain of the amplifier results in even

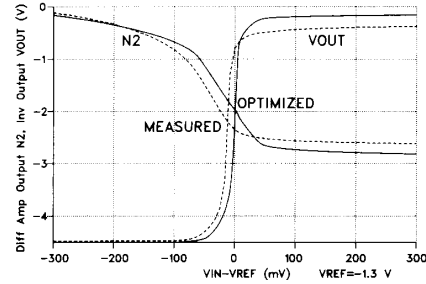


Fig. 14. Simulated and measured DMC transfer characteristics with 100K ECL levels. Measured results with 100K ECL levels are shown with the dashed lines for the differential-amplifier output and the inverter output. Simulated solid-line characteristics are with optimized device sizes.

smaller total input offset voltage and a larger net effective signal.

D. Simulated and Measured DMC Transfer Characteristics with 100K ECL Levels

To test for 100K ECL capability, measured transfer characteristics for the same typical DMC receiver measured for Fig. 13 are plotted in Fig. 14 (dashed line) with 100K ECL levels. The dynamic range of the amplifier is adequate to accommodate this 0.7-V increase upward in common-mode voltage. However, an adjustment in the device size design, as shown by the solid-line nominal simulation, improves the operation and leaves more margin for worst-case conditions. This change in device sizes degrades the gain of the differential amplifier and increases the input offset voltage by about 30 percent. Nevertheless, the net signal for the worst-case example is still adequate to drive the inverter output to on-chip CMOS levels.

V. CMOS RECEIVER DELAY

Due to the use of only one stage of differential amplification and minimum channel-length design in critical devices, while meeting the 100-mV worst-case sensitivity specification, any access-time penalty for using ECL receivers instead of TTL receivers is small. Plotted in Fig. 15 is the simulated and measured receiver delay as a function of input signal amplitude relative to the reference. The DMC receiver in 1- μm technology and with the device sizes shown in Fig. 4 is the top curve. The curve shown is nearly identical to that for the SD and DD receiver with the device sizes shown in Figs. 3 and 5. Even with the worst-case net signal of about 50 mV found from the example analysis, the receiver delay is 2 ns. Nominal

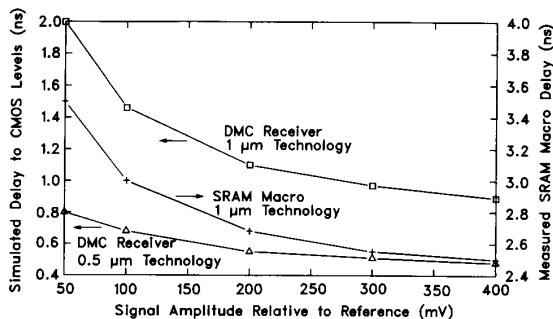


Fig. 15. CMOS receiver delay. Simulated receiver delay is shown as a function of single-rail input signal amplitude. Measured delay is also shown for a 64K SRAM macro, which includes logic functions and development of drive for a 4-pF load.

parameters were used in this simulation. However, the worst-case net signal occurs for shorter than nominal channel-length input devices, which would result in less than nominal delay. Variations in channel length and threshold on the short-channel input devices have a dominant impact on both speed and input offset voltage, tending to minimize delay variations around nominal.

The delay shown in Fig. 15 is reasonable relative to the TTL receiver delay included in the 10–25-ns nominal access times reported for SRAM in 1- μ m technology. Also, there is a delay savings relative to TTL at the off-chip driver due to the smaller signal swings required for ECL. Thus, any net increase in access time for going from asynchronous TTL interfaces to asynchronous ECL interfaces should be minimal. If dual-rail input signals are available for the critical path, considerably less than 1-ns receiver delay is possible.

As an example of an actual application, the delay for a 64K SRAM chip-select clock macro, with the DD receiver used as the input stage and with the Table IV parameter variations, is shown on Fig. 15. This is a complex macro, which includes delay for logic and for development of drive for a 4-pF load. The increase in delay with signal amplitude, however, is all in the receiver stage and is close to that predicted by simulation. For optimum macro delay in this particular application, an inverter four times larger than shown in the schematic (Fig. 3) loads the differential-amplifier input stage. As demonstrated by the SRAM macro curve, the differential amplifier withstands this larger load without a significant increase in the delay delta with decreasing signal amplitude.

The comparison between the DMC receiver delay simulation in 1 μ m [10] and the result in 0.5 μ m [11] is also shown in Fig. 15. This 0.5- μ m receiver is IBM ECL power supply compatible. Important here is not only the improvement in delay but also the improvement in best-to-worst-case delay delta.

VI. CONCLUSIONS

CMOS ECL receiver circuits consisting of a differential-amplifier first stage and a CMOS-inverter second stage are shown to supply on-chip CMOS levels after the second stage. The amplifiers feature built-in feedback compensa-

tion for common-mode parameter variations, large interleaved input devices for minimizing the impact of differential mismatches, and minimum channel-length design on critical devices for speed.

Simulated and measured results for 5-V 1- μ m technology demonstrate feasibility for better than 100-mV worst-case sensitivity. No access time penalty or only a small one should be incurred in going from TTL interfaces to ECL interfaces, depending on the details of the actual application.

In the submicrometer regime, small-signal interfaces are in even more demand for high-speed systems. The lower power supply, higher gain and speed, and lower magnitude of parameter variations relative to the input signal amplitude will result in still higher speeds at the receiver relative to the total access time and in smaller worst-to-best-case variations. We have used these high-speed CMOS ECL receivers in sub-10-ns 64K SRAM designs in both 1- μ m and submicrometer technologies.

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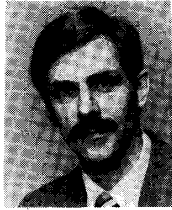
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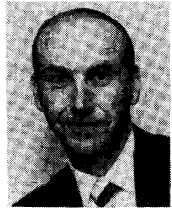
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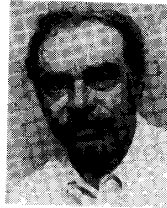
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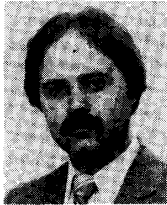
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