

ECE 733
Midterm Spring 2009

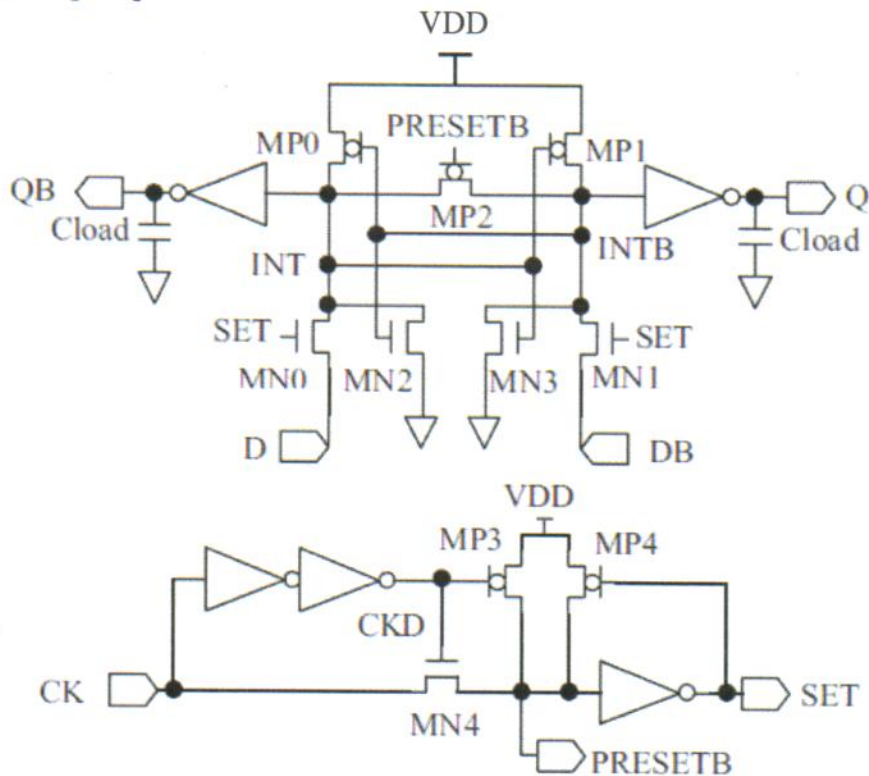
Name: Solutions
 Student Number: _____
 Section Number: 001 / 601

The exam is open book, open notes. No computers are permitted. **90 minutes.**

Write your name and student number on top of this sheet of paper and turn that in. Please write your answer in the space provided after each question. Note there is space to expand on any multiple choice answers.

Question 1

Consider the flip-flop below.

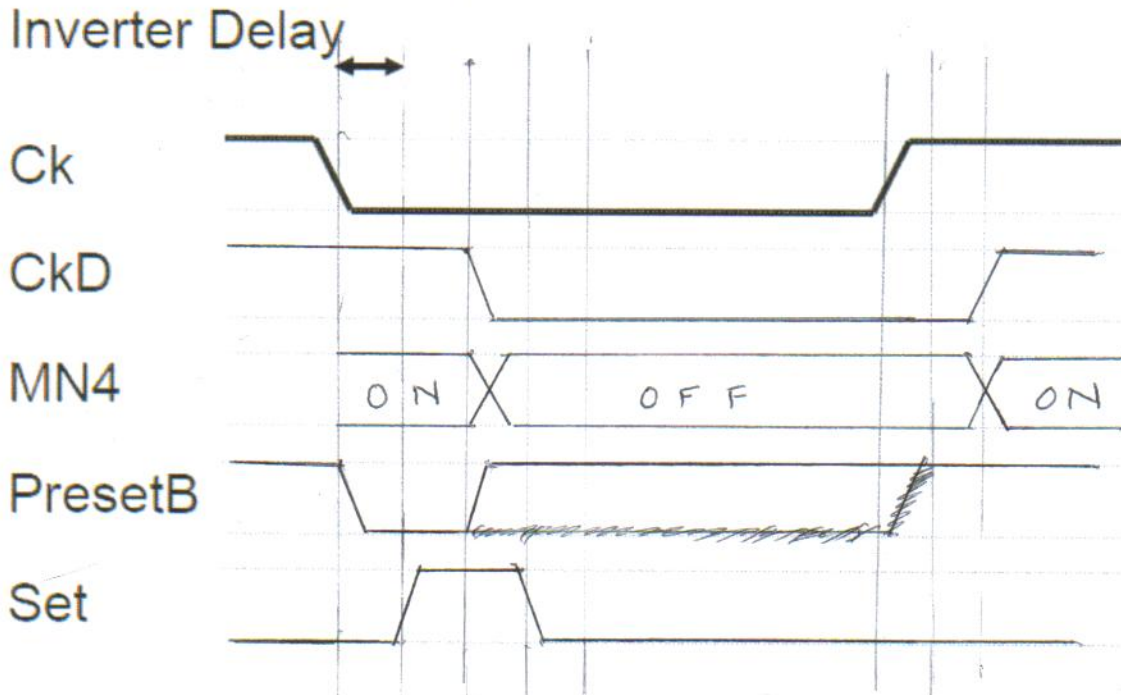


Please answer the following questions:

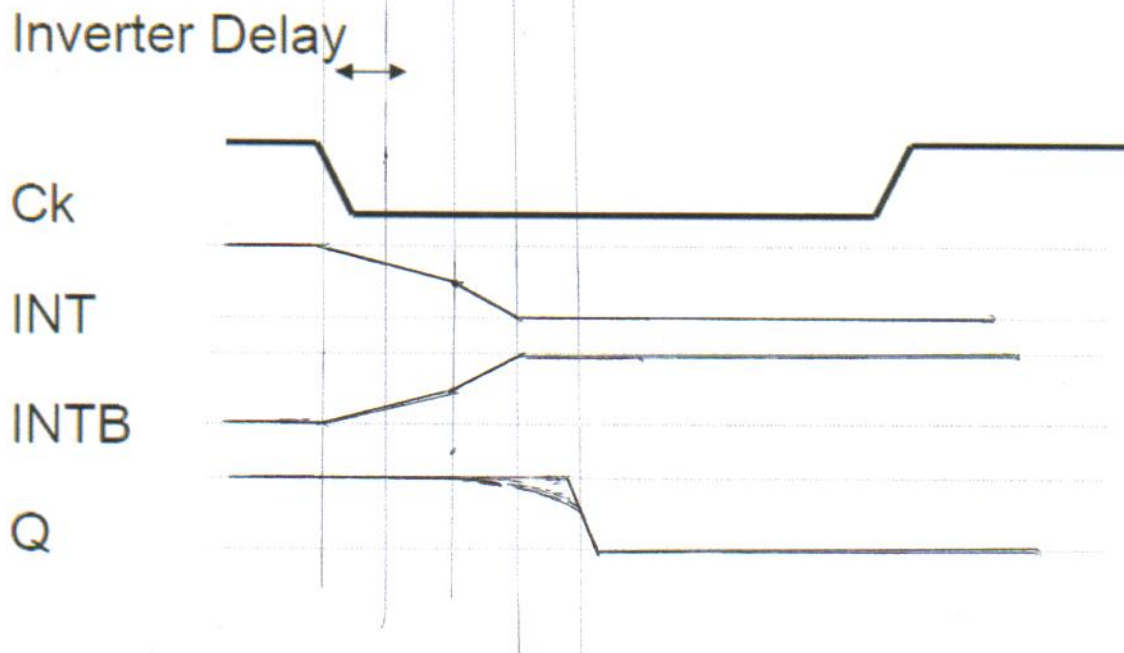
(a) Is this a Master Slave or pulsed flip-flop? [1 point]

Pulsed

(b) Show the waveforms and relative timing of the following signals and transistor states to do with the circuit at the bottom of the figure. Notice the scale bar indicating the period equal to an inverter delay. Signal names are not case sensitive. The dotted grey lines show V_{DD} and Gnd. [4 points]



(c) To the same scale show the waveforms with the initial conditions INT = 1, INTB = 0, D = 0, DB = 1. [4 points]



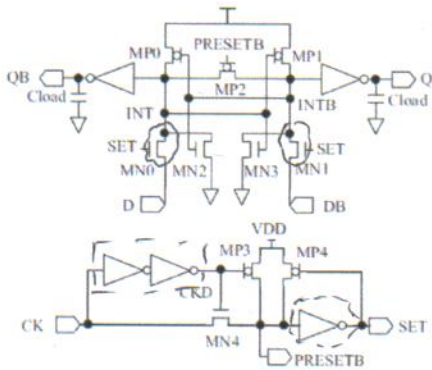
— During Preset INT & INTB are equalized close to $V_{DD}/2$.

(d) How is the state of the cross-coupled inverter that forms the latch changed? There is ONE correct answer. Explain the reason for your choice clearly. [2 points]

- A. It is overcome by in sampling transmission gate and associated inverters.
- B. Regeneration is effectively broken during sampling of the input. The inputs do not have to overcome a stable state.**
- C. It is a dynamic latch.
- D. The latch is precharged to logic 1 before sampling.

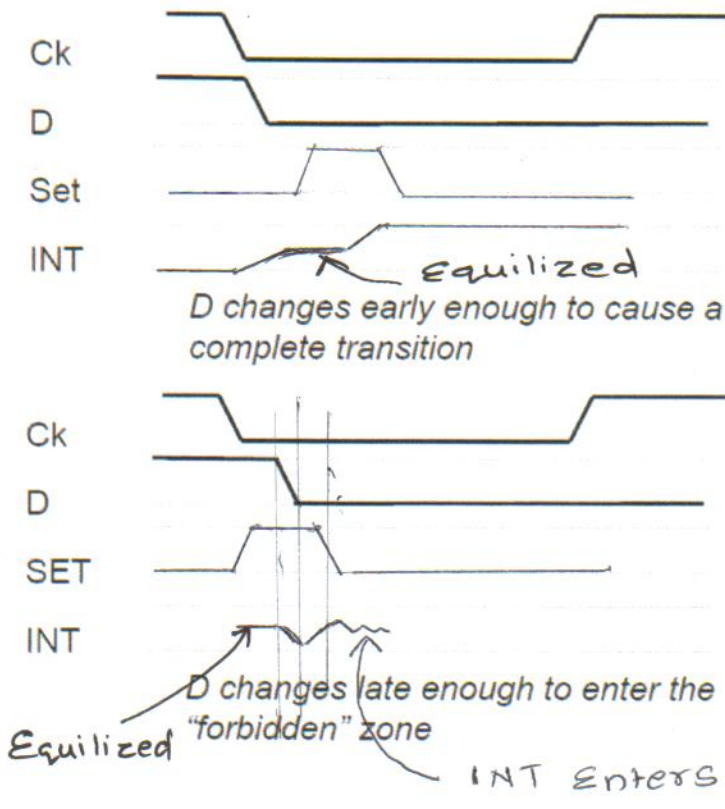
B. MP2 equalizes during Preset.

(e) What transistors and factors determine the set up time? Explain your answer – just don't circle transistors. Use the timing diagram. [4 points]



- Time to turn on/off SET transistors
- Time taken by latch to transition sufficiently.
- Delays from CLK to SET.

Inverter Delay



During SET, INT starts transition. If D changes too late into set, INT won't have enough time to reverse transition sufficiently.

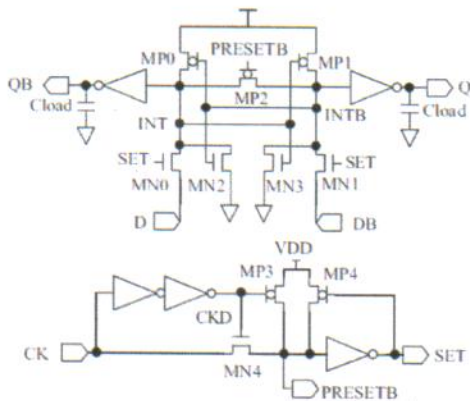
(f) Is the set-up time positive or negative? [1 point]

Negative. As set comes after clock edge.

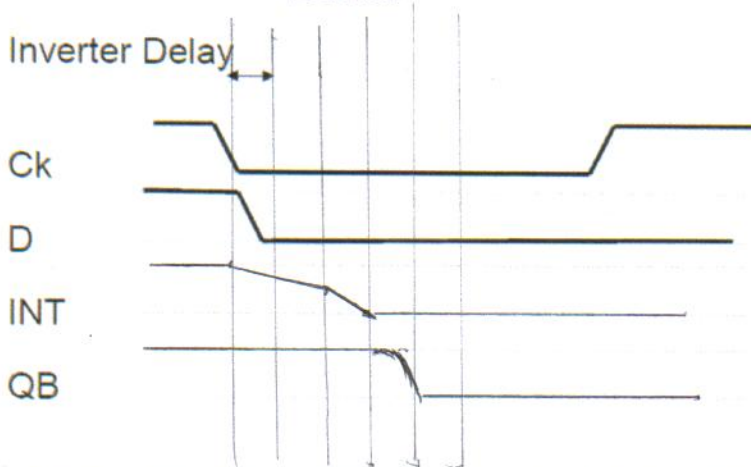
(g) What is the role of transistor MP2? What benefit does it bring to the circuit? [2 points]

- Equilizes latch, bringing it to neutral state.
- Speeds up $t_{\text{mux} \rightarrow Q}$
- Makes the latch ratio-insensitive.

(h) What delays determine $t_{\text{ck} \rightarrow Q}$? Explain your answer clearly, using the timing diagram. [2 points]



- Delays to SET.
- Internal delay to latch to a fixed state.
- Delay in o/p inverter.



(i) For the same size inverters, is the sampling window in this flip-flop, narrower, wider or the same, as the sampling window in the HLFF? [2 points]

Narrower. This circuit has 2 inverters wide window. HLFF has it 3 inverter wide.