

ECE 733
Quiz 2 Spring 2011

Name:

Student ID:

This test is open book, open notes. Computers, PDAs and cell phones are NOT allowed (calculators are). You have 60 minutes. Turn in answers in the space provided.

Question 1

When and why is it important to include on-chip inductance when modeling high speed clock distribution networks? How is it modeled?

Question 2

What are the sources of random jitter in chip to chip links and what can be done to reduce their impact on the bit error rate (BER)?