ECE 733
Final Spring 2006

This test is open book, open notes. Computers are NOT allowed (calculators are). You have 75 minutes. Turn in answers on your own paper.

Question 1
Consider the following cross-section for an interconnect circuit:

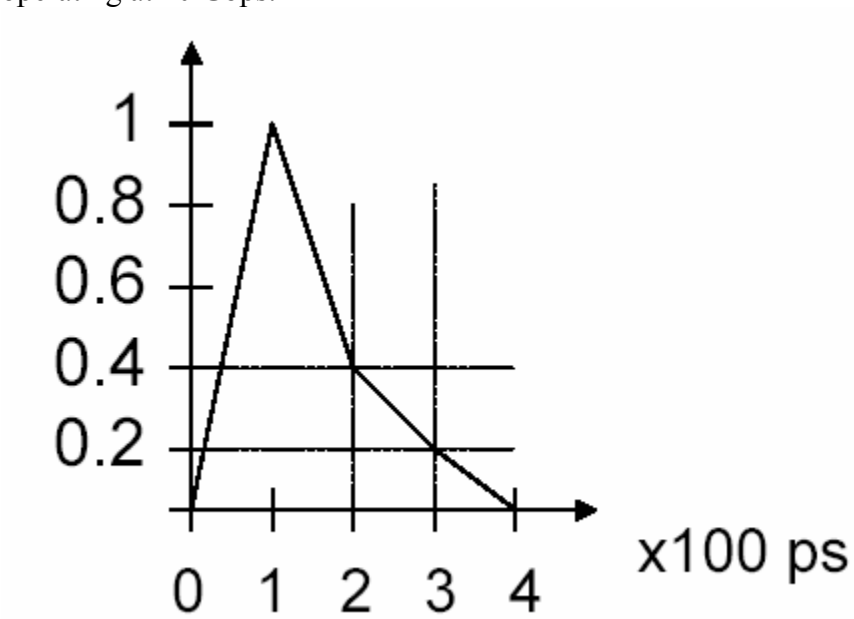
- Line width = 10 um; Line thickness = 2 um
- Line material: Aluminum (ρ = 4.3E-8 Ω.m)
- Dieletric material : BCB. ε_r=2.7; tan δ = 0.0008
- $\mu = 4\pi$E-7 (Magnetic permeability)
- Z0= 50 Ohm

(a) At what frequency is the skin-depth half of the conductor thickness? [2 points]

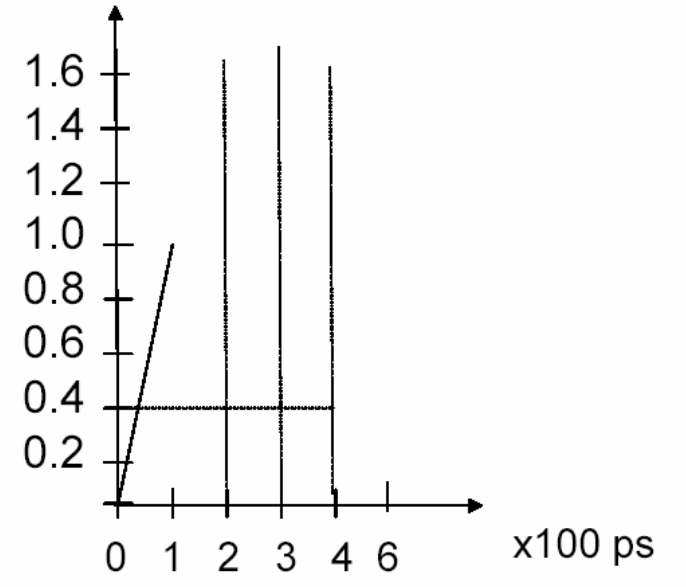
(b) At what frequency does the attenuation due to the loss tangent exceed the attenuation due to the skin effect? [3 points]

(c) Would you get the best Bit Error Rate by using PAM-2 or PAM-4 as your signaling scheme on this line? Carefully explain your answer. [2 points]

Question 2
Consider an interconnect circuit with the following pulse response to a 010 input operating at 10 Gbps.

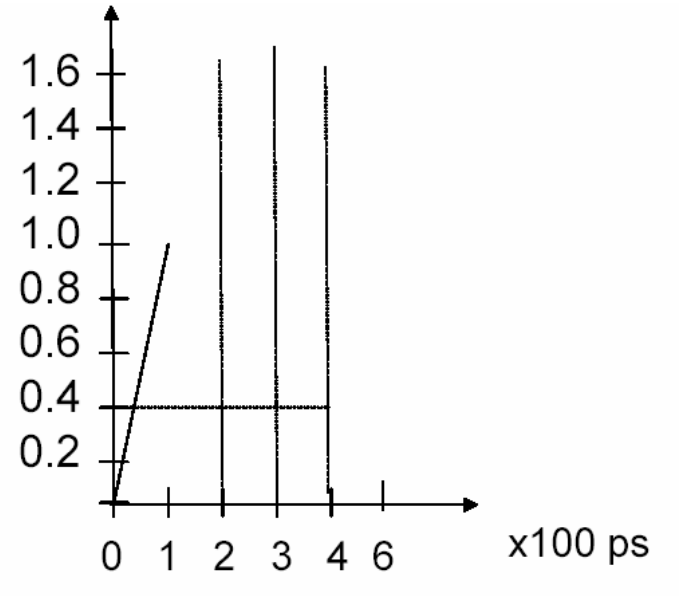


(a) Based on this waveform, predict the waveform for a 0110 signal operating at 10 Gbps, as it would appear at the end of the same line. [4 points]



(b) How many taps (i.e. how many flip-flop delays) would you use in a pre-emphasis filter, and what are appropriate tap weights. [3 points]

(c) Draw the waveform at the end of the line for a 0110 signal operating at 10 Gbps, as produced by the driver with the filter. [2 points]



Question 3

Consider the 8T cell, considered in the distributed paper, and described below:

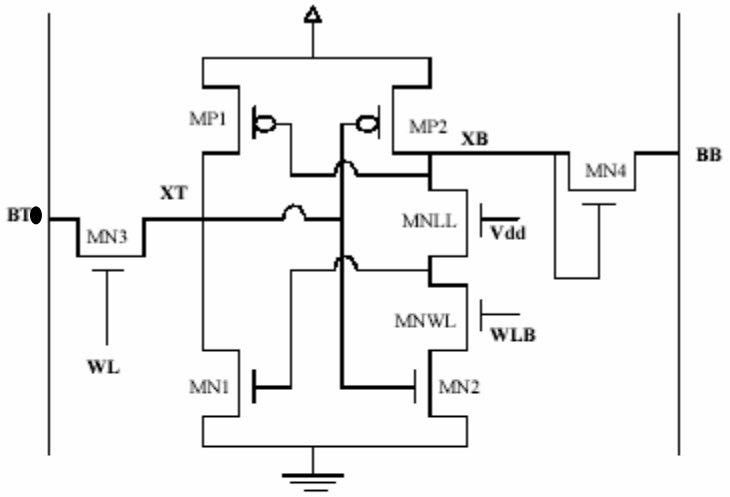


Figure 2. 8T SRAM Cell

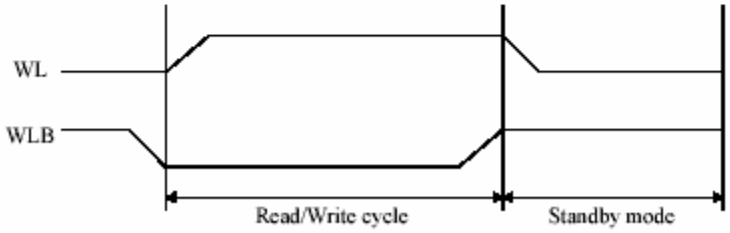


Figure 3. Timing Diagram

Please answer the following questions:

(a) What are the constraints, if any, on the relative sizes of MN1 and MN3 to read a "0" stored at XT without upsetting the state of the memory? Clearly justify your answer. [2 points]

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(b) For the SRAM to work correctly, it needs to ensure that when reading a stored "1", then (BT,BB) = (1,0) must be met, and for reading a stored "0", that (BT,BB)=(0,1) must be met. What potential issues do you see driving BB→ 0 if XB is low? Thus, how should the column "load" circuits be redesigned to ensure correct operation? [2 points]