ECE 733
Final, Spring 2006

This test is open book, open notes. Computers are NOT allowed (calculators are). You have 75 minutes. Turn in answers on your own paper.

Question 1
Consider the following cross-section for an interconnect circuit:

- Differential pair.
- Line width = 10 um
- Line thickness = 2 um
- Line Separation = 20 um
- Line material: Aluminum (ρ = 4.3E-8 Ω.m)
- Dieletric material : BCB. ε_r=2.7; tan δ = 0.0008
- μ = 4πE-7 (Magnetic permeability)
- Z0= 50 Ohm

(a) At what frequency is the skin-depth half of the conductor thickness? [2 points]

$$f_s = \frac{\rho}{\pi\mu(t/2)^2} = 10.9GHz$$

(b) At what frequency does the attenuation due to the loss tangent exceed the attenuation due to the skin effect? [3 points]

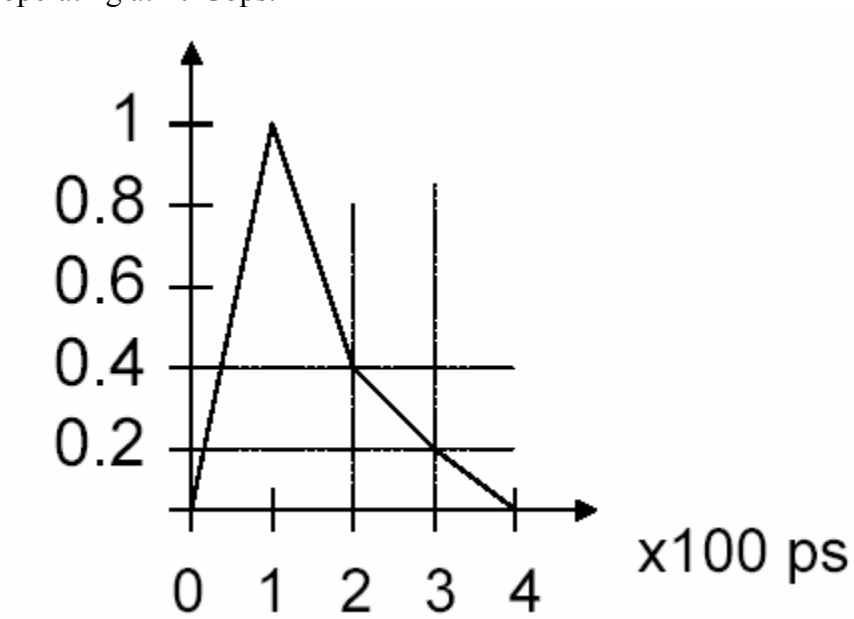
$$\alpha_D = \frac{\pi f\sqrt{\varepsilon_R}\tan\delta_D}{c} = 1.37E-11*f \qquad \alpha_s = \frac{R_{DC}}{2Z_0}\sqrt{\frac{f}{f_s}} = \frac{2150}{100}\sqrt{1/10.9E9}\sqrt{f} = 2.06E-4\sqrt{f}$$

225 THz! (2.25E14 Hz)

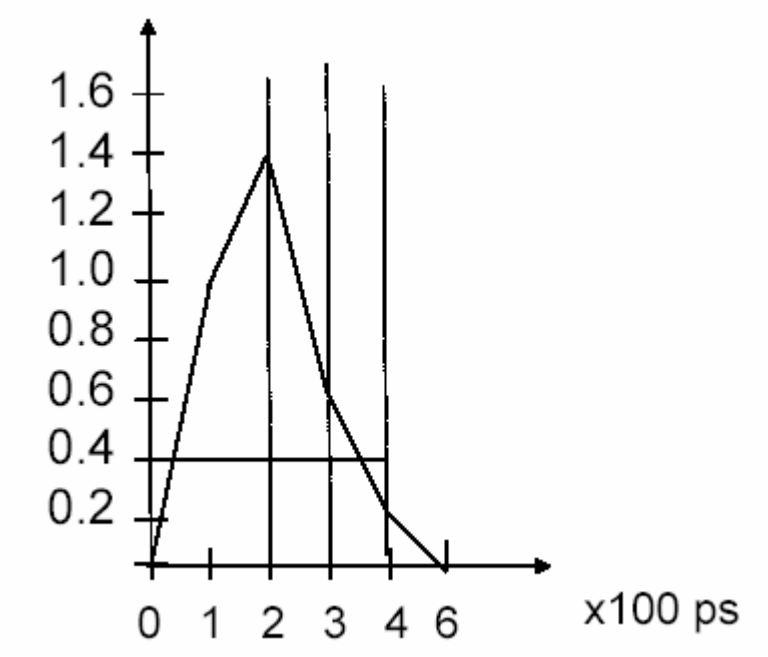
(c) Would you get the best Bit Error Rate by using PAM-2 or PAM-4 as your signaling scheme on this line? Carefully explain your answer. [2 points]

PAM-2, as the frequency roll-off of loss is small.

Question 2
Consider an interconnect circuit with the following pulse response to a 010 input operating at 10 Gbps.



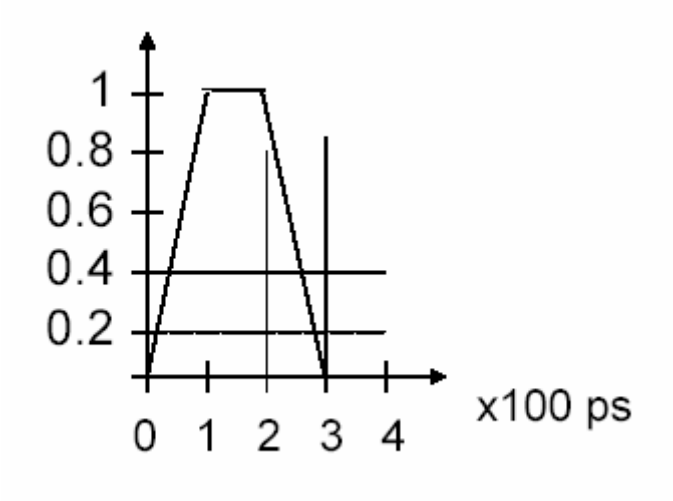
(a) Based on this waveform, predict the waveform for a 0110 signal operating at 10 Gbps, as it would appear at the end of the same line. [4 points]



(b) How many taps (i.e. how many flip-flop delays) would you use in a pre-emphasis filter, and what are appropriate tap weights. [3 points]

2, 0.4, 0.2

(c) Draw the waveform at the end of the line for a 0110 signal operating at 10 Gbps, as produced by the driver with the filter. [2 points]



Question 3

Consider the 8T cell, considered in the distributed paper, and described below:

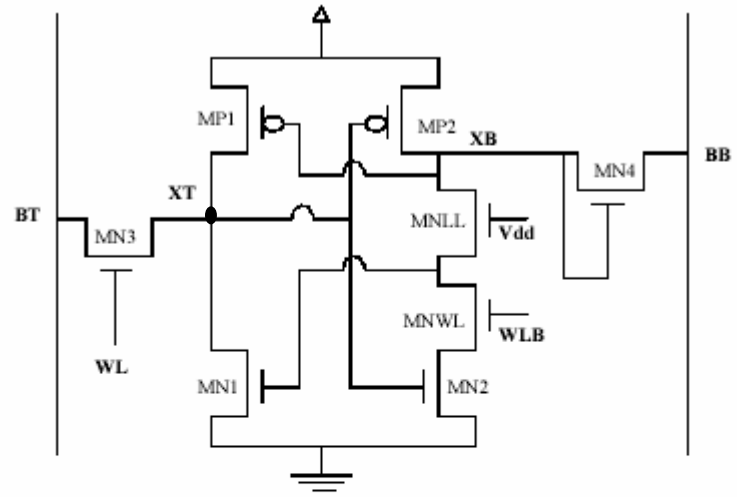


Figure 2. 8T SRAM Cell

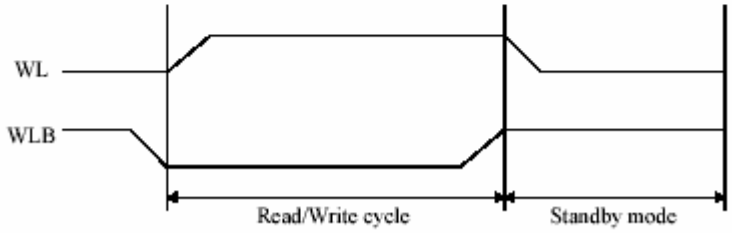


Figure 3. Timing Diagram

Please answer the following questions:

(a) What are the constraints, if any, on the relative sizes of MN1 and MN3 to read a "0" stored at XT without upsetting the state of the memory? Clearly justify your answer. [2 points]

No constraint, as MNWL=off prevents a logic change.

(b) For the SRAM to work correctly, it needs to ensure that when reading a stored "1", then (BT,BB) = (1,0) must be met, and for reading a stored "0", that (BT,BB)=(0,1) must be met. What potential issues do you see driving BB→ 0 if XB is low? Thus, how should the column "load" circuits be redesigned to ensure correct operation? [2 points]

This question was changed in the exam – ignore. A range of answers were accepted.