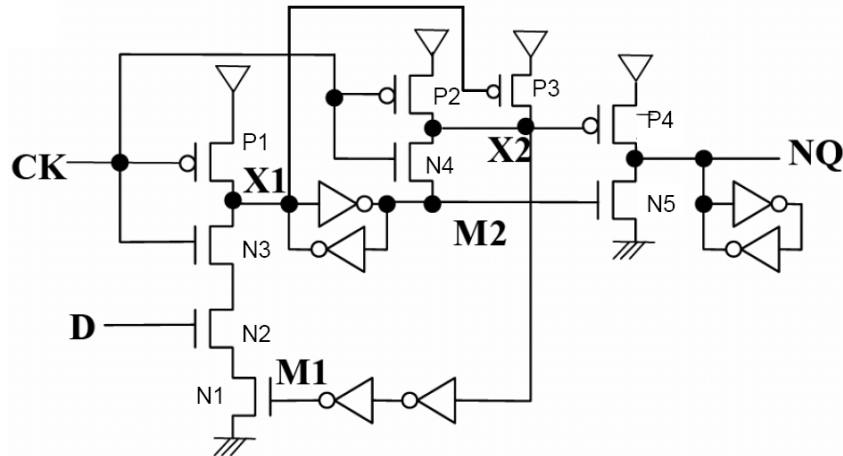


ECE 733
Final Spring 2007

This test is open book, open notes. Computers are NOT allowed (calculators are). You have 75 minutes. Turn in answers on your own paper.

Question 1

Consider the circuit below, the Cross Charge Coupled Flip-flop (XCFF), a variant of the SDFFF.



Please answer the following questions:

(a) When $Ck=0$, which nodes are precharged and are they pre-charged high or low? (2 points)

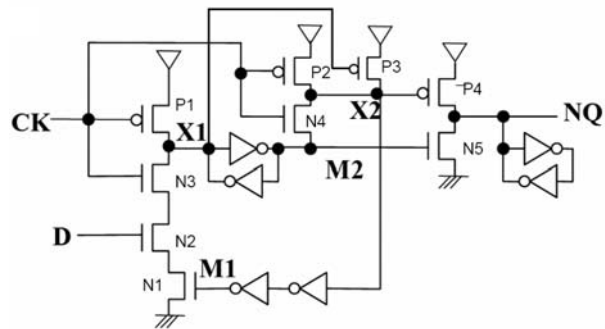
$$X1=X2=1$$

(b) After precharge, what is the basic operation as Ck goes from 0 to 1 and if $D=1$? Clearly label which transistors are on and what the values of nodes $X1$, $X2$, M , $M2$ and NQ are after $ck \rightarrow 1$. What is the critical path? (4 points)

$X1$ pulled low;
 $M2$ pulled high;
 $X2$ stays high;
 $NQ=0$.

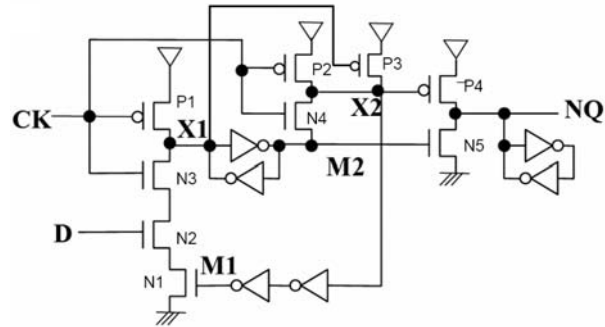
On: $N1, 2, 3, 4, 5, P3$

$N1-2-3$, Inv, $N5$



(c) After $Ck \rightarrow 1$, what happens if D changes from 1 to 0? I.e. Why does the flip-flop state not change? (2 points)

N2 goes off, leaving X1 driven low by latch.
Everything else stays same.

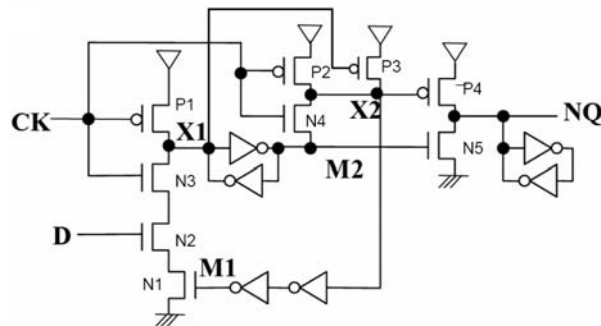


(d) After precharge, what is the basic operation as Ck goes from 0 to 1 and if D=0? Clearly label which transistors are on and what the values of nodes X1, X2, M, M2 and NQ are after $ck \rightarrow 1$. What is the critical path? (4 points)

X1 stays high, so M2 stays low. N4 turns on, pulling X2 down. $NQ=1$.

On: N4, P4

N4 through P4



(e) After the transition in part (d), what prevents a false transition if D changes to 1 while clock is high? [2 points]

X2 is 0 so N1 is off.

(f) What is the purpose of transistor P3? Does it need to be big or small? [2 points]

Keep X2 high when D=1.
Small

(f) How does the capacitive load on X1 and X2 compare with that on X in the SDFF? (1 point)

X1, X2 Lower

Question 2

Please answer the following short questions.

(a) Of the following loss mechanism, which has the most impact on a 5 Gbps channel? DC resistance, skin effect, dielectric loss, or voltage sharing due to a series termination resistance. [2 points]

Dielectric loss

(b) Why is a run-length code still desirable in DC-connected channels? [2 points]

Give enough edges to enable clock recover

(c) For the following data input, which is the expected waveform after going through a standard pre-emphasis filter with one tap flip-flop. [4 points]

