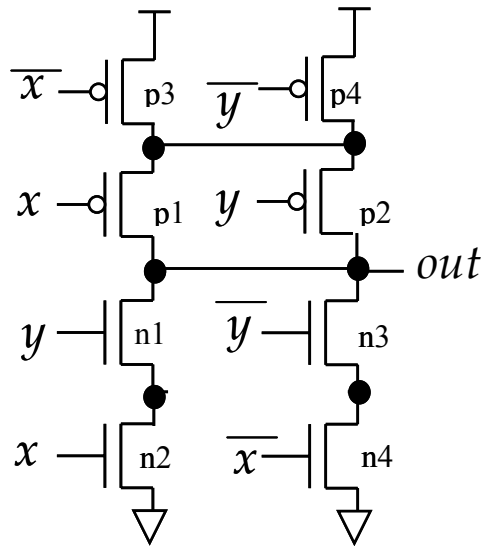


ECE 733
Midterm
Spring 2004
P. Franzon

Make sure to enter your name and student # on the scan sheets. Use a pencil on the scan sheets. There are **13** questions.

Consider the following gate for questions 1-4:



Question 1

What is the logic function implemented by this gate?

- A. $Out = x.y + x'.y'$
- B. $Out = x.y' + x'.y$
- C. $Out = x.y + x'.y$
- D. $Out = x.y' + x.y'$
- E. None of the above

Question 2

If $\mu_n = 2\mu_p$, and we ignore second order effects, what transistor sizing would give equal rise and fall times, symmetric noise margins, and the fastest worst case delay? All inputs will change at the same time.

- A. All minimum size transistors
- B. $W_{n1} = W_{n2} = W_{n3} = W_{n4} = 1$; $W_{p1} = W_{p2} = W_{p3} = W_{p4} = 2$;
- C. $W_{n1} = W_{n3} = 1$; $W_{n2} = W_{n4} = 2$; $W_{p1} = W_{p2} = 2$; $W_{p3} = W_{p4} = 4$;
- D. $W_{n1} = W_{n3} = 2$; $W_{n2} = W_{n4} = 1$; $W_{p1} = W_{p2} = 4$; $W_{p3} = W_{p4} = 2$;
- E. These alternatives all give the same timing

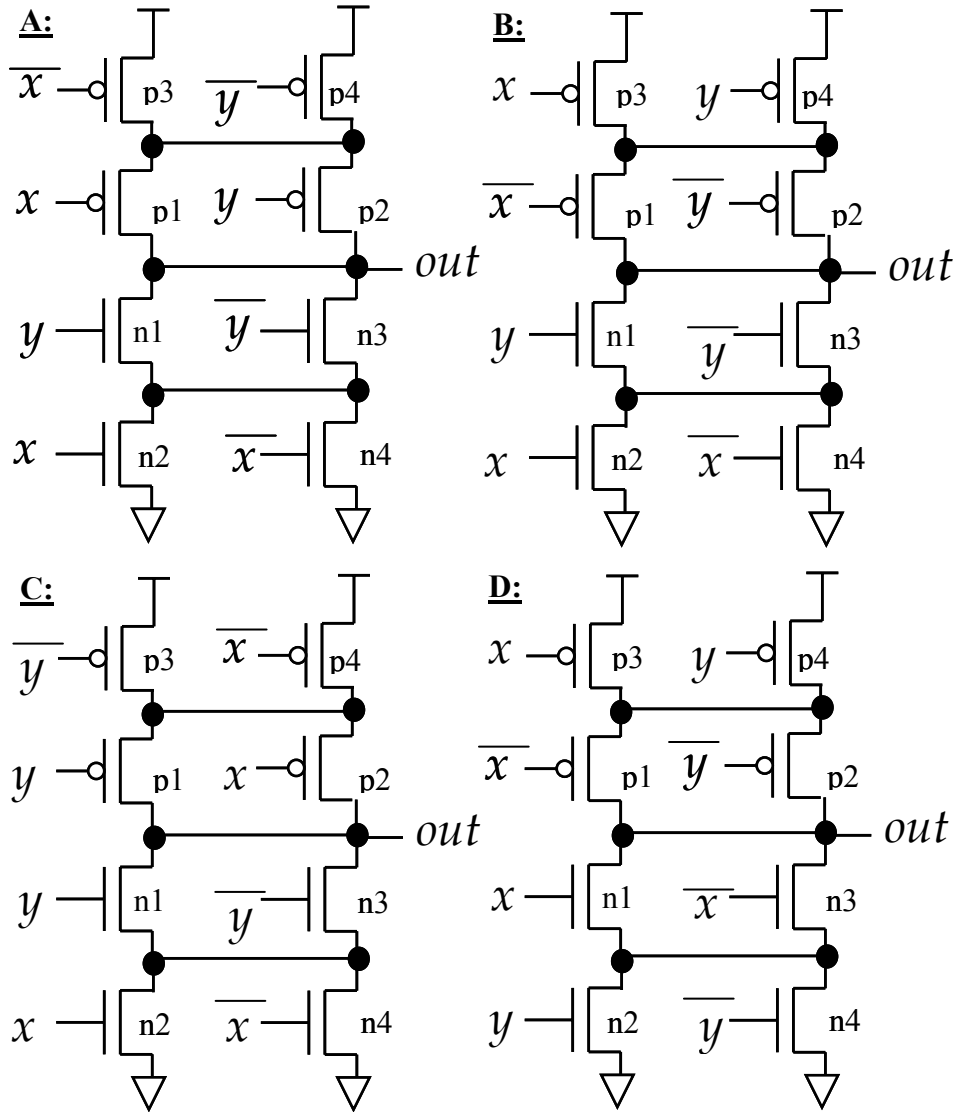
Question 3

If $\mu_n=2\mu_p$, what transistor sizing would give the lowest power solution. All inputs will change at the same time.

- A. All minimum size transistors
- B. $W_{n1} = W_{n2} = W_{n3} = W_{n4} = 1$; $W_{p1}=W_{p2}=W_{p3}=W_{p4} = 2$;
- C. $W_{n1}=W_{n3}=1$; $W_{n2} = W_{n4} = 2$; $W_{p1} = W_{p2} = 2$; $W_{p3}=W_{p4}=4$;
- D. $W_{n1}=W_{n3}=2$; $W_{n2} = W_{n4} = 1$; $W_{p1} = W_{p2} = 4$; $W_{p3}=W_{p4}=2$;
- E. These all give the same power consumption.

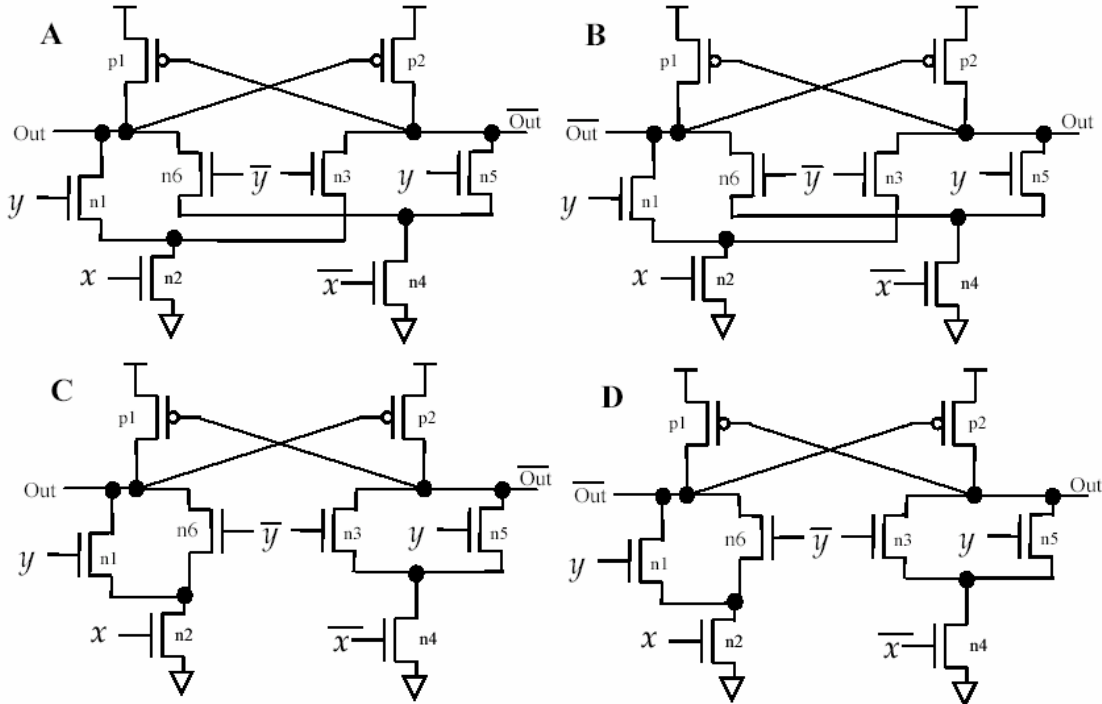
Question 4

If x changes later in the clock period than y , which design would lead to the average fastest delay through the gate, assuming minimum sized transistors.



Question 5

Which gate is the DCVS version with the equivalent logic function to the gate used in Questions 1-4 (note that the correct placement of the pins out and out' matters)?



E. None of these

Question 6.

How are the pFETs sized in the DCVS gate and why ($\mu_n=2\mu_p$)?

- A. They are usually sized the same as the nFETs, as the pFET size does not impact circuit performance significantly.
- B. They are made larger than the nFETs so as to minimize rise time.
- C. They are made smaller than the nFETs so that the latter's pull down effect can quickly overcome the pFET pull up effect.
- D. They are made smaller than the nFETs as there are 2 nFETs in series.
- E. None of these statements are correct.

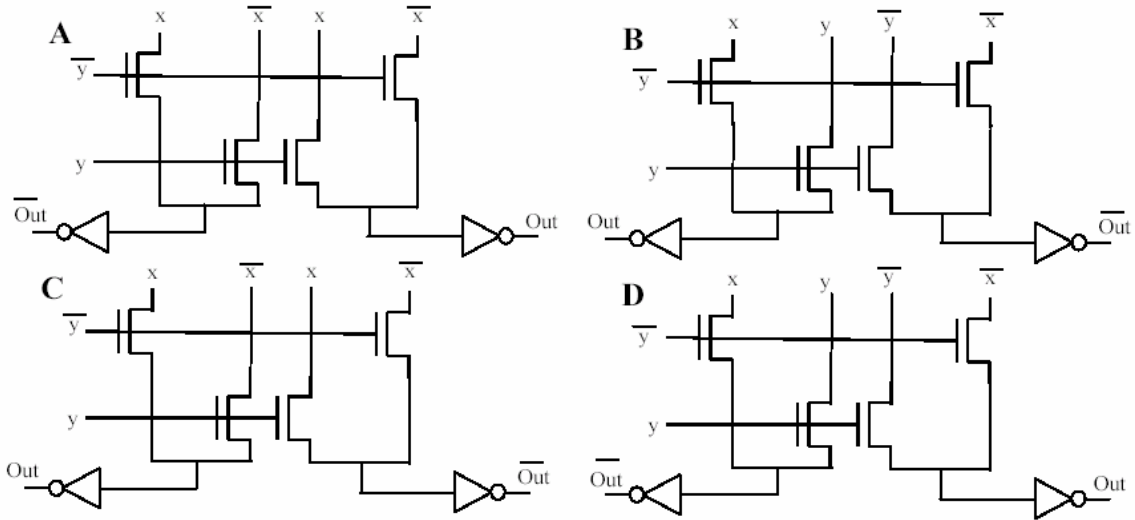
Question 7.

What nFET sizes might you choose in the DCVS logic so as to minimize the difference between the worst and best case delay through the gate?

- A. $W_{n2}=W_{n4}=1$; $W_{n1}=W_{n6}=W_{n3}=W_{n5}=2$;
- B. All minimum size.
- C. $W_{n2}=W_{n4}=3$; $W_{n1}=W_{n6}=W_{n3}=W_{n5}=2$;
- D. $W_{n2}=W_{n4}=10$; $W_{n1}=W_{n6}=W_{n3}=W_{n5}=10$;
- E. None of the above.

Question 8

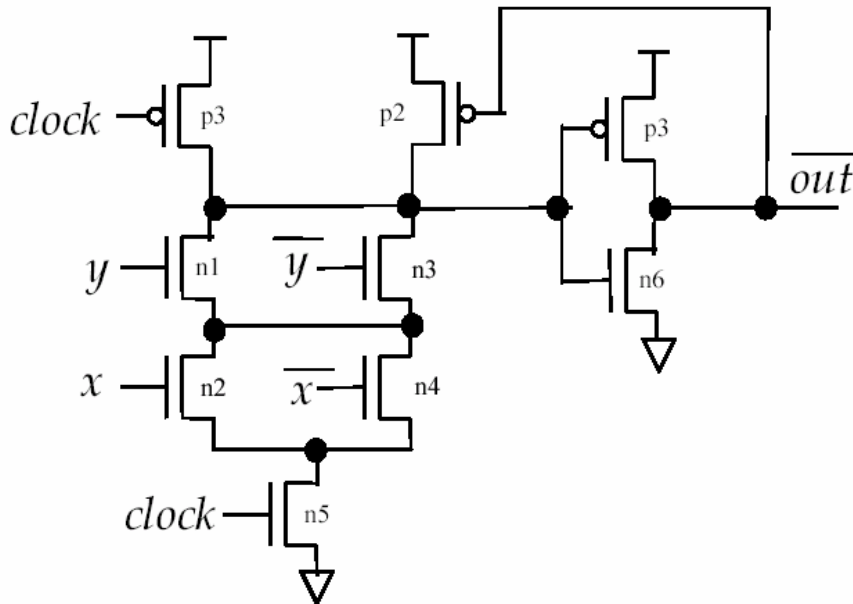
Which topology provides the CPL equivalent to the logic gate function presented in Questions 1-4 (note that the correct placement of the pins out and out' matters)?



E. None of the above

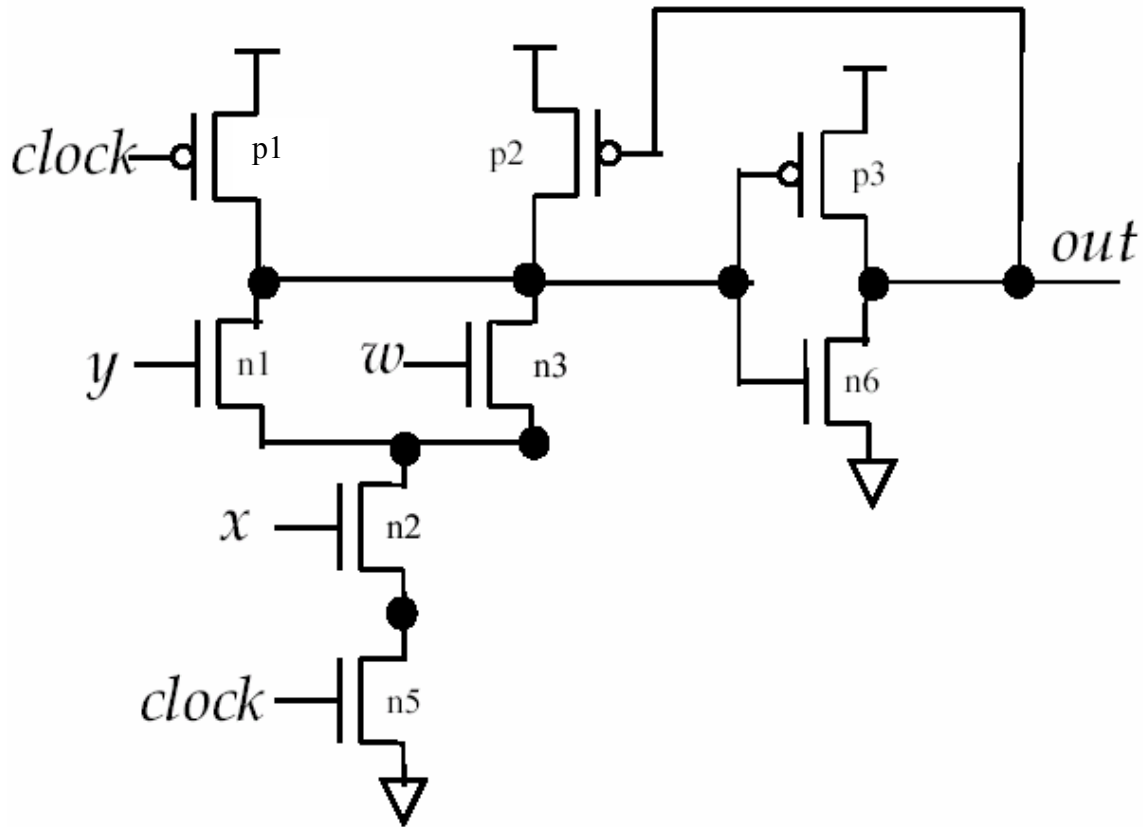
Question 9

Would you consider implementing the logic function implied in questions 1 to 3 with the following Domino logic gate, in order to get a dynamic logic implementation? (Take care in your answer, consider all the design issues for domino logic.)



- A. Yes
- B. No

The next few questions apply to the following Domino logic gate:



Question 10

What logic function is implemented?

- A. $out = w.x.y$
- B. $out = x.(w+y)$
- C. $out = (w.x.y)'$
- D. $out = (x.(w+y))'$
- E. None of the above.

Question 11

Precharge transistor p1 is sized so that:

- A. W_{p1} is small so that the nFETs can overcome it.
- B. W_{p1} is large so that it can overcome the nFETs.
- C. If the clock duty cycle (t_{high}/t_{period}) is around 50%, then $W_{p1} \approx W_{n1}$ (or even smaller) might be a good starting point for design consideration.
- D. If the clock duty cycle (t_{high}/t_{period}) is around 50%, then it makes sense to make W_{p1} as large as you can, while considering clock load issues.
- E. None of the above arguments leads to a good size for W_{p1} .

Question 12

The keeper p2 is used to pull up the internal node in case of a charge sharing event (e.g. n1 or n3 turn on while n2 stays off). Would the voltage drop on a charge sharing event be reduced if we swap n1 and n3 with n2 (i.e. place n1 and n3 in parallel below n2, and connect the drain of n2 to the drain of p2).

- A. Yes
- B. No
- C. There would be no difference

Question 13

The inverter n6/p3 is sized with what primary consideration?

- A. To make the noise margin at the input to the inverter n6/p3 symmetric (NML=NMH)
- B. To give equal rise and fall times at the output.
- C. To turn off p2 at a relatively high voltage, if the pull down chain provides a path to ground.
- D. All of the above are equally important.
- E. None of the above are important.