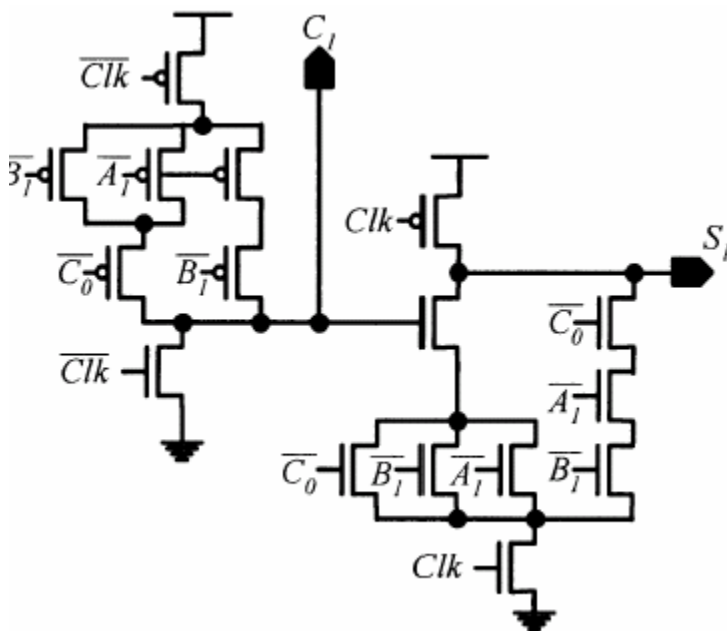


ECE 733
Midterm
Spring 2005
P. Franzon

This test is open book, open notes. Computers are NOT allowed (calculators are). You have 75 minutes. Answer in the space provided.

Question 1

Consider the following gate:



Please answer the following questions:

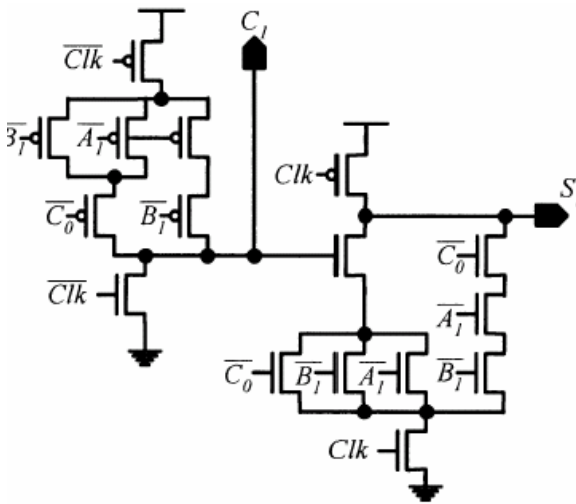
(a) To what class of logic does this gate type belong (e.g. “DCVS”)? (1 point)

(b) When are C1 and S1 pre-charged and when are they evaluated? (2 points)

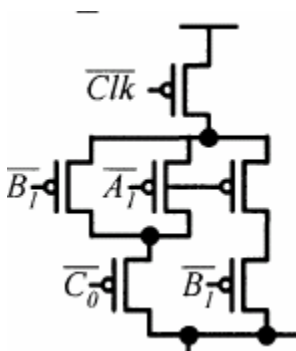
(c) Write the logic expression for C1. What is its function (in words)? (3 points)

(d) What is the DC noise margin HI and LO on input A1? Ignore the body effect. (2 points)

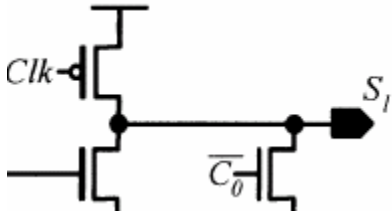
(e) If the transistors are all the same size, what is the critical path to S1 from the inputs? Use the figure in your answer. Clearly identify which transistors are in this path, and the order in which they might turn on. (4 points)



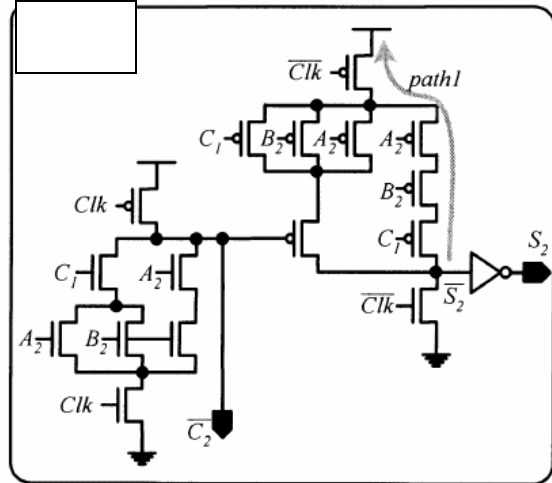
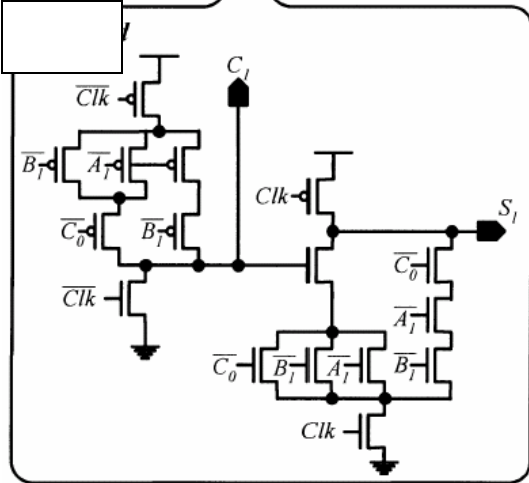
(f) Let's speed up this circuit. If you had only 3 pFET sizes, $w=10$, $w=8$, and $w=6$, how would you assign them to the transistor group below?



(g) Which of the two nFETs below need to be larger to speed up the critical path? (1 point)

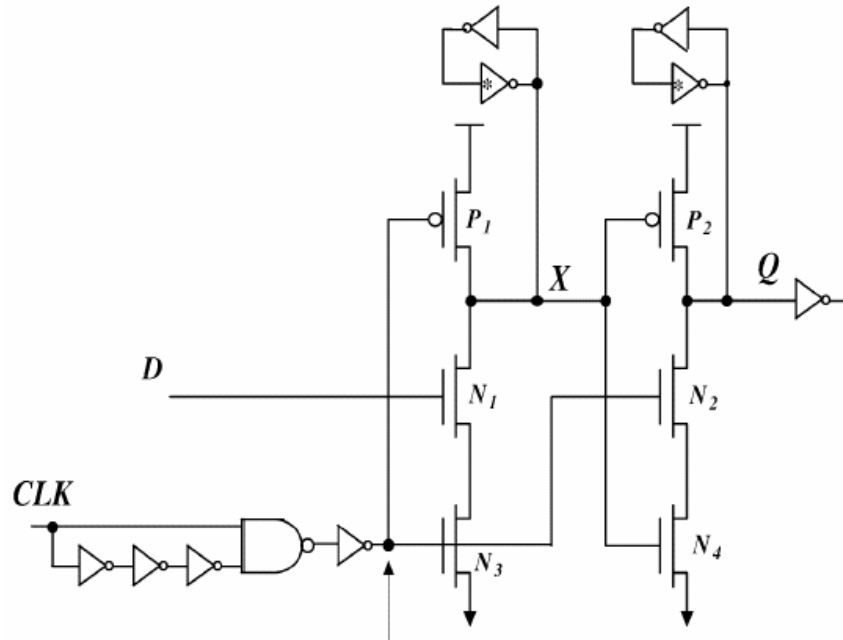


(h) C1 drives the next stage shown on the RHS below. If all transistor sizes are the same, what possible error can occur at S2' (s2 bar) for the inputs A1B1C0=111 and A2B2=00? (5 points)



Question 2

Consider the following circuit.



(a) Is this a Master Slave or pulsed flip-flop? (1 point)

(b) Is this single-edge or double-edge sampled? (1 point)

(c) Explain the operation of this flip-flop, using the example of $D=1$. Show a waveform for a complete clock period, including CLK, D, X and Q in your waveform. [5 points]

(d) If D goes to 0 after CLK goes low, what prevents Q from changing incorrectly? [2 points]