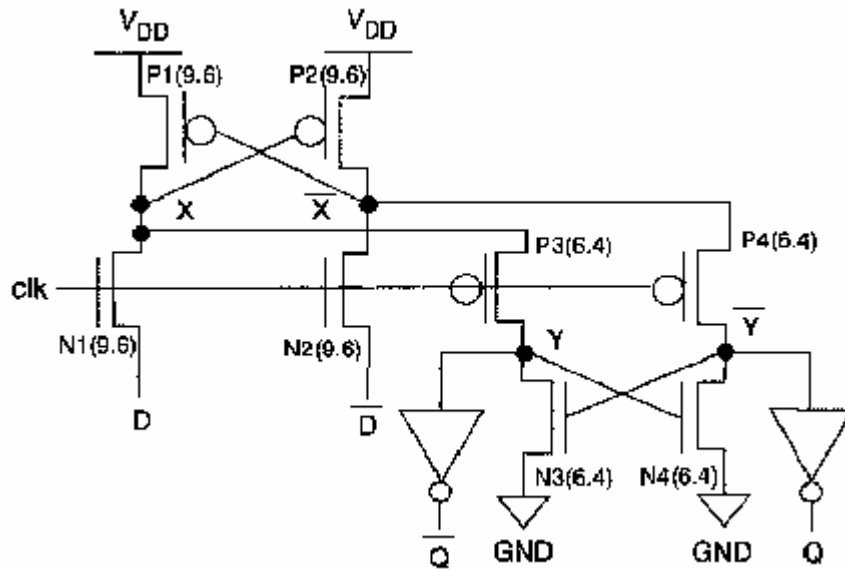


**ECE 733**  
**Midterm Spring 2006**

This test is open book, open notes. Computers are NOT allowed (calculators are). You have 75 minutes. Turn in answers on your own paper.

**Question 1**

Consider the following pass-gate flip-flop:



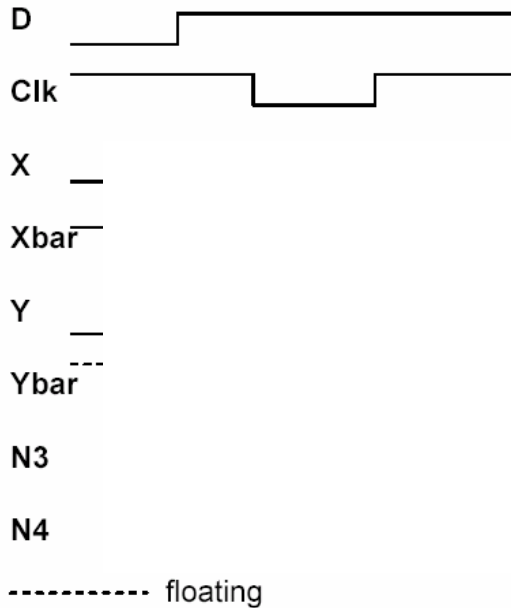
Please answer the following questions:

(a) Is this a static or dynamic (pre-charged) flip-flop? (1 point)

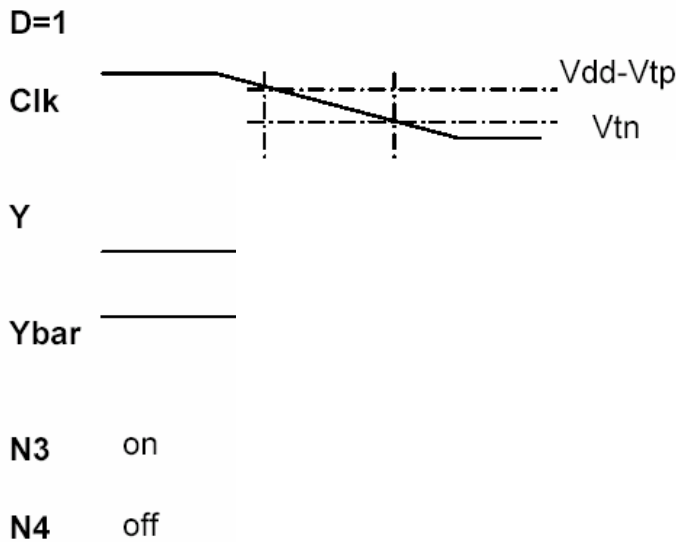
(b) Is this a pulsed or Master-Slave flip-flop? (1 points)

(c) If  $D=1$  while  $Clock=1$ , is the voltage at X equal to  $V_{DD}$  or  $V_{DD}-V_t$ ? (1 point)

(d) Complete the following timing diagram, showing the approximate voltages, the states (on/off) of the transistors N3, and N4, and which nodes are floating and when. Note Y is initially 0. To get all 4 points, the times when Y/Ybar are floating must be correctly identified as well as the transistor states, as well as the logic values of Y and Ybar. (4 points)



(e) For this 0 → 1 transition, (X=1, Y=0 initially) show detail as to which changes first, Y or Ybar, and when they change with respect to other waveforms cross  $V_t$ . i.e. Describe the detailed timing operation of the circuit in the diagram **as well as in words**. It is important to describe the exact sequence of Y and Ybar changing voltage, and N3 and N4 changing state (on/off). There are the 4 items to get correct for each of the 4 points. (4 points)



- (f) Describe in words, what voltage is required at node Y just after the clk changes from 1 to 0 and thus what must be the relative sizes of transistors P1, P3 and N3 for correct operation. (3 points)
- (g) Show how this gate would be redesigned so that it has the input logic  $A \oplus B$  (A XOR B). i.e. It stores  $A \oplus B$  when clk transitions High to Low. Make sure to use complementary pass gate logic. (3 points)
- (h) What will determine the set up and hold time for this flip-flop? (2 points)
- (i) What prevents Q from changing if D changes after the clock transition is complete? (1 point)