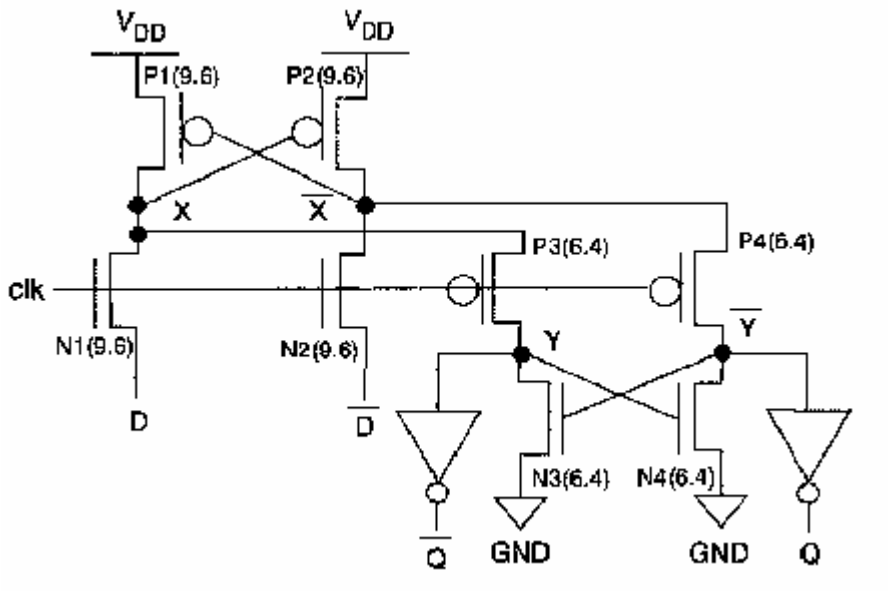
ECE 733
Midterm Spring 2006

This test is open book, open notes. Computers are NOT allowed (calculators are). You have 75 minutes. Answer in the space provided.

Question 1
Consider the following pass-gate flip-flop:



Please answer the following questions:
(a) Is this a static or dynamic (pre-charged) flip-flop? (1 point)

Static.

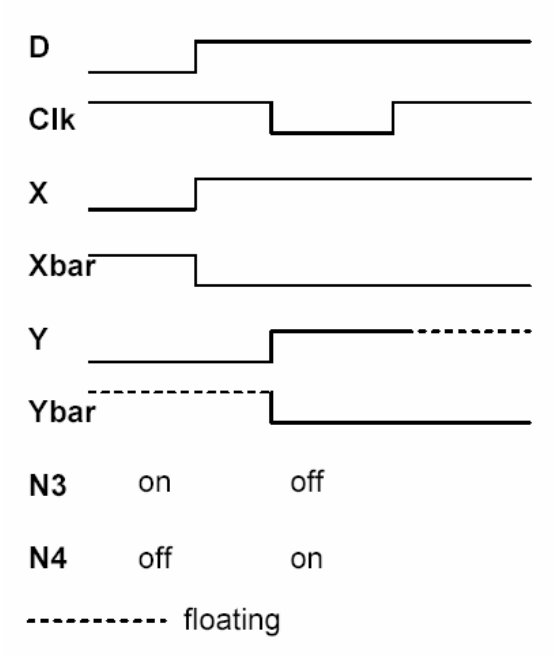
(b) Is this a pulsed or Master-Slave flip-flop? (1 points)

Master-Slave

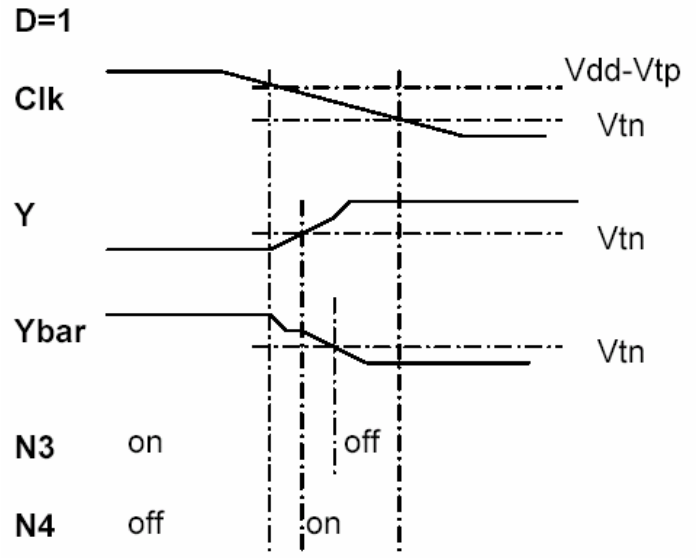
(c) If D=1 while Clock=1, is the voltage at X equal to Vdd or Vdd-Vt? (1 point)

Vdd, as P1 will be on.

(d) Complete the following timing diagram, showing the approximate voltages, the states (on/off) of the transistors N3, and N4, and which nodes are floating and when. Note Y is initially 0. To get all 4 points, the times when Y/Ybar are floating must be correctly identified as well as the transistor states, as well as the logic values of Y and Ybar. (4 points)



(e) For this 0 → 1 transition, (X=1, Y=0 initially) show detail as to which changes first, Y or Ybar, and when they change with respect to other waveforms cross Vt. i.e. Describe the detailed timing operation of the circuit in the diagram **as well as in words.** It is important to describe the exact sequence of Y and Ybar changing voltage, and N3 and N4 changing state (on/off). There are the 4 items to get correct for each of the 4 points. (4 points)

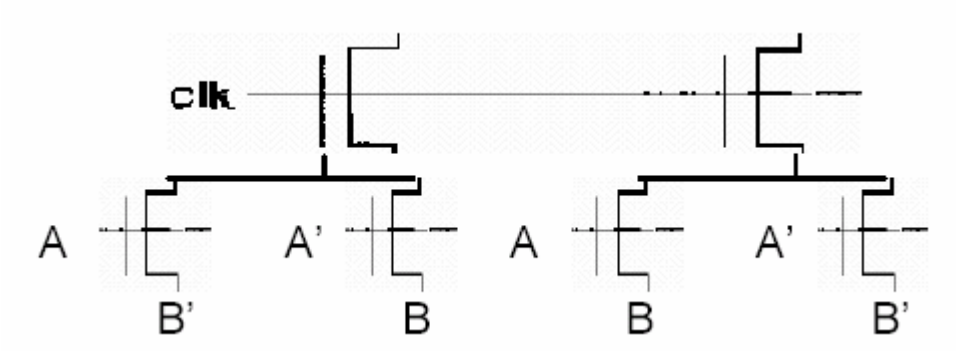


When p3/p4 go on,
Y starts getting pulled Hi.
As soon as it exceeds Vt,
It starts turning N4 on, pulling
Ybar low, which in turn turns
N3 off.

(f) Describe in words, what voltage is required at node Y just after the clk changes from 1 to 0 and thus what must be the relative sizes of transistors P1, P3 and N3 for correct operation. (3 points)

V_Y must exceed Vtn so that it can turn on N4. Thus P1 and P3 must be large enough to pull up Y while N3 is on.

(g) Show how this gate would be redesigned so that it has the input logic A^B (A XOR B). i.e. It stores A^B when clk transitions High to Low. Make sure to use complementary pass gate logic. (3 points)



(h) What will determine the set up and hold time for this flip-flop? (2 points)

How long it takes N1 and N2 to transmit any change in D to X, and how long it takes to turn off (which depends on the clock slope).

(i) What prevents Q from changing if D changes after the clock transition is complete? (1 point)

The transistors N1 and N2 are off.