NC STATE UNIVERSITY

ECE 712: Integrated Circuits for Wireless Communications

Instructor:
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Course web page http://moodle.wolfware.ncsu.edu/course/view.php?id=34393
****Please use the course bulletin board to ask questions about lectures, HW, projects, etc. It is the best way to broadcast questions that may be of interest to everyone.*

Course Objective:
After taking this course, the student will be able to analyze and design the key integrated circuits found in modern silicon radio receivers, transmitters, and frequency synthesizers.

Course Description:
Topics will include the following: silicon IC technology choices, integrated active and passive components, RF amplifiers, noise, Gilbert-cell mixers, phase-locked loops, and voltage-controlled oscillators. Homework and projects will make use of Cadence / SpectreRF design tools.

Prerequisites:
Required: ECE 511 Analog Electronics
Strongly encouraged: ECE 549 RF Design for Wireless

Required Text:
- Recommended:
  Behzad Razavi, *RF Microelectronics*, 2nd edition, Prentice Hall, New Jersey, 2012
- Alternate:
  Thomas Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2nd edition, 2004.

Supplementary Texts:
- Floyd Gardner, *Phaselock Techniques*, Wiley, 3rd edition, 2005
- Gray, Hurst, Lewis, and Meyer, *Analysis and Design of Analog Integrated Circuits*, Wiley, 5th edition
- Michael Steer, *Microwave and RF Design*, SciTech Publishing, 2010.

Grading:
25% Test 1
25% Test 2
20% Homework (roughly 7 assignments)
30% Design project (1 design projects)

Planned Course Outline:

I. Context
   1. Overview of wireless communications
   2. Radio architectures

II. Lumped-Element Networks
   1. RLC networks, matching, Q
   2. On-chip passive components

III. Distributed-Element Networks
   1. Transmission Lines
   2. Scattering Parameters
   3. Smith charts

IV. Active Components
   1. Single-stage amplifiers
   2. RF transistors, figures of merit

V. Noise Analysis

VI. Low-Noise Amplifiers
   1. Noise parameters
   2. Gain, NF, linearity
   3. Unilateral design methodology

VII. Nonlinear Circuit Analysis

VIII. Mixers
   1. Active topology: Gilbert cell
   2. Passive topology, N-path filtering

IX. Voltage-controlled oscillators
   1. Fundamentals
   2. Phase noise
   3. Cross-coupled oscillator design

X. Phase-Locked Loops
   1. Fundamentals
   2. Linear analysis
   3. Noise analysis

XI. Power Amplifiers
   1. Class of operation
   2. Linearity and efficiency

Students with Disabilities:
Reasonable accommodations will be made for students with verifiable disabilities. To take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Hearth Center, Campus Box 7509, 515-7653. http://www.ncsu.edu/dso.

Audit Students:
Any student auditing the course is expected to maintain a B average or better on all homework assignments. Audit students do not have to complete design projects.

Academic Integrity:
Students should refer to the University policy on academic integrity found in the Code of Student Conduct (found in Appendix L of the Handbook for Advising and Teaching). *It is the instructor's understanding and expectation that the student's signature on any test or assignment means that the student neither gave nor received unauthorized aid.* Authorized aid on an individual assignment includes discussing the interpretation of the problem statement, sharing ideas or approaches for solving the problem, and explaining concepts involved in the problem. Any other aid would be unauthorized and a violation of the academic integrity policy. Any computer work submitted must be completed on your own personal computer or from your own NCSU account to avoid confusion about the origin of the file, and no sharing of files in any way is allowed.

Design Projects:
A design project is planned for this course. Students will be creating designs using available industry design kits and Cadence / SpectreRF design tools. The overall grading of the project will depend upon the quality and content of the design report and the performance of the design against specifications.

→**Late policy**: design projects must be submitted on-line before 11:55PM on the due date. Late submissions will automatically incur a 20% penalty PLUS an additional 1% per day late.

Homework:
Approximately 6 homework assignments will be assigned through the course of the semester, accounting for 20% of the grade.

→**Late policy**: late homework will automatically incur a 20% penalty and must be submitted no later than the end of the weekend the week they are due.