

# Monolithic Copper Integrated Circuitry supporting Multi-layer Micro-Electro-Mechanical Systems

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In the majority of MEMS processes, polysilicon is the dominant mechanical material and silicon dioxide is the dominant sacrificial material. In this SRC process, however, Copper is the mechanical material and the remaining nitride and silicon dioxides are utilized as the sacrificial layers. To create freely moving Copper mechanical structures, the sacrificial layers must be removed from the film stackup. This process, or series of processes, is known collectively as the "release."

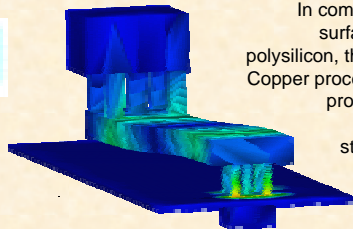
To successfully remove the 11 layers of sacrificial material from this Copper process, etchants were identified that have controllable etch rates and high selectivity to the material they remove. Hydrofluoric acid is known to etch silicon dioxides selectively, and etch rates can be controlled by varying the concentration. Phosphoric acid, at a temperature of 180°C and a concentration of 85%, is known to etch silicon nitride. Though a series of alternating steps, we hope to remove the eleven layers of sacrificial material necessary to release three mechanical layers of copper.

Because exact film thickness and compositions are not known at this time, etch rates are difficult to predict. For this reason, a series of test structures were included in the layout which allow accurate determination of film thicknesses using a spectrometer. In addition, other test structures will be used to monitor the effect of our etchants on the mechanical copper layers. In this manner, any corrosive effects can be quantified and hopefully minimized.

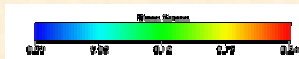
## Variable-Depth Cu Release Recipe: Alternating materials act as etch stops Tunable design tradeoff of layers Mechanical complexity vs. non-mechanical wiring density



**New High-V Device:**  
•Extended Drain PMOS ("SVX" technique.)

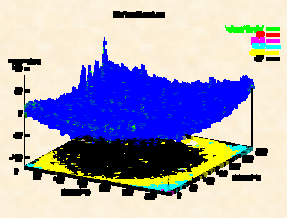


In comparison to common surface micromachined polysilicon, the electrodeposited Copper process has potential to provide greater design complexity, lower stress (and therefore lower drive voltages), and better VLSI integration.



## Establishing Design Guidelines for future CuMEMS Designers

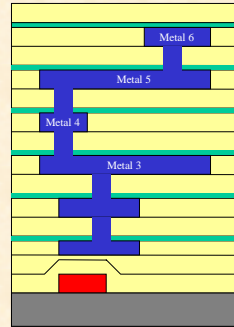
### Typical polySi-based MEMS post-release mirror flatness



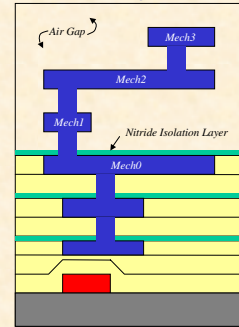
An important step in the design of MEMS devices within a new process is the accurate characterization of strain fields and inherent properties in the mechanical material. Differences between thermal expansion coefficients of stacked thin films are a primary source of stresses across the films. These associated strain fields can cause bending and buckling of the mechanical layers once the sacrificial oxides are removed. Another important property to characterize is the Young's modulus of the copper thin films. Used in calculating resonance frequencies for many MEMS devices, including mirror pistons, accurate determination of the Young's modulus for these films is required to calculate device characteristics such as switching speeds.

## Develop Post-processing Recipe for Controlled Release of Surface Micromachines

### As Delivered from UMC:



### After Multistage Release:



Micromachining involves the release of material structures by selectively etching chosen sacrificial materials (dielectric and nitride) from what become the electro-mechanical layers (metal). As the number of released metal layers is increased, so too is the potential complexity of the resulting mechanical system. With only one (1) mechanical layer, designers limited to building deformable beams and membranes (just as in bulk micromachining). With two (2) mechanical layers, fixed hinges and axles can be created. Three (3) layers allows for free (horizontal or vertical) translation of those two-layer devices (e.g., for a crank-arm). And four (4) mechanical layers allows for translatable gears on shared axles.

### Process Monitor Structures (not shown)

- Under-etch (intersecting cavities)
- Over-etch and Material Selectivity
- Stiction (cantilever beams)

## Copper-based Advantages:

**Unprecedented VLSI-MEMS seamless integration for microsystem array development in a standard process (no lateral separation of definition areas, as in M<sup>3</sup>S, iMEMS, or SmartMUMPs)**

**Simultaneous multi-level capability in both mechanics and wiring (MEMS are typically either poly-Si w/ single metal, or Single laminated stack of Al-dielectric-Al)**

**Potential for smallest-ever electromechanical elements (ala damascene planarity and low-stress vias)**