4 Gbps High-Density AC Coupled Interconnection

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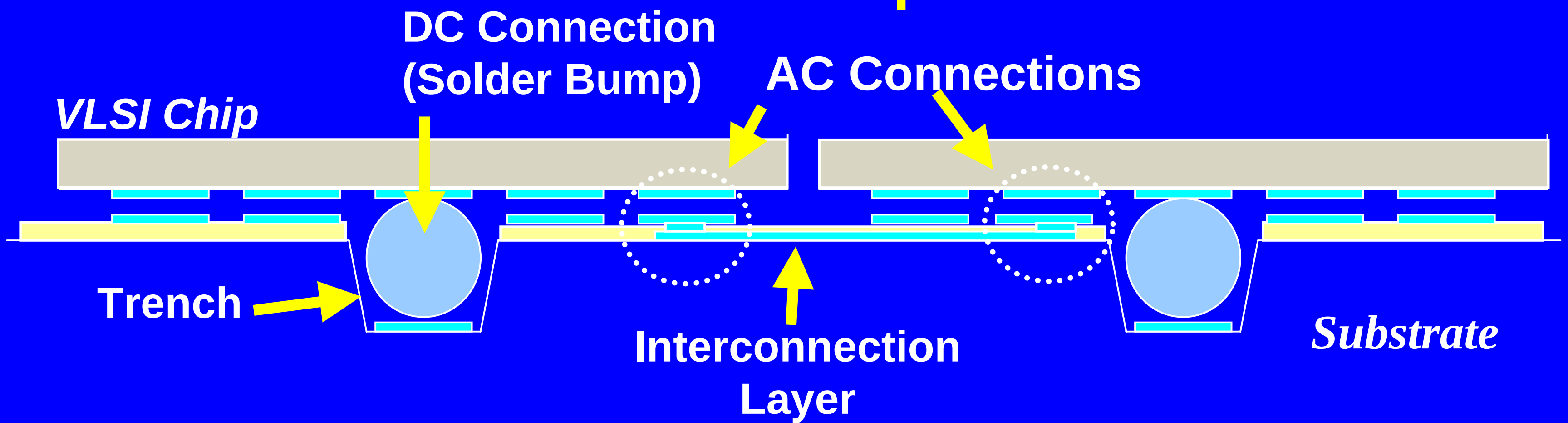
Outline

- Concept and Benefits
- Physical Structure
- Capacitive Coupling
- Inductive Coupling
- Discussion & Future Work

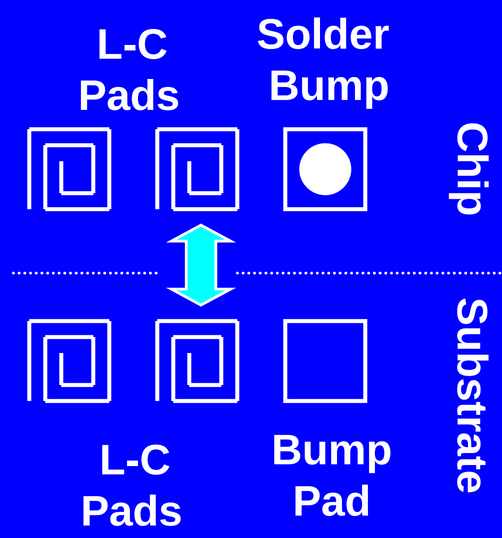
AC Coupled Interconnect

Concept and Benefits

AC Coupled Interconnect Concept

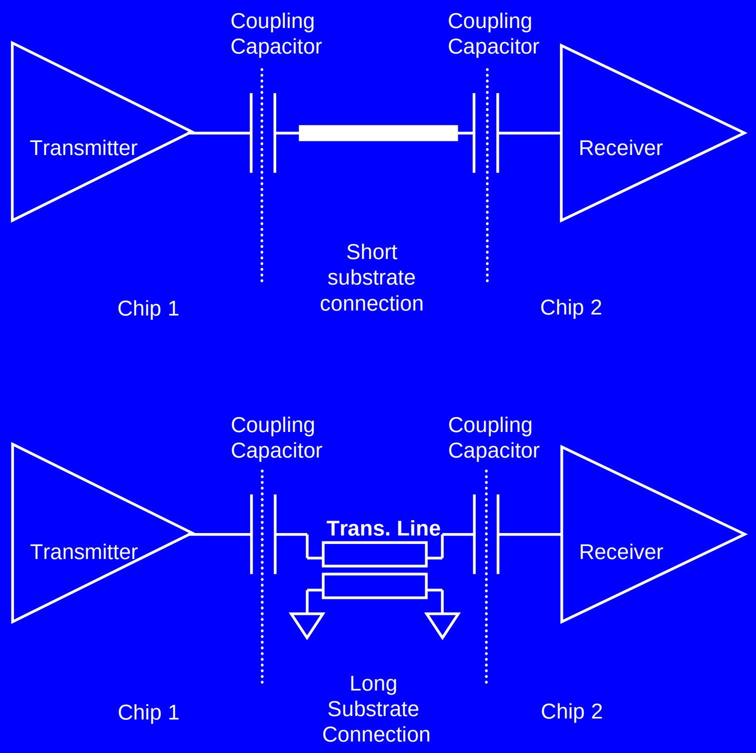


- AC coupled connections down to 70 µm pitch on large scale arrays
- Signaling through capacitive or inductive coupling
- Buried solder bumps to bring chips into proximity and provide DC power
- High-speed, low-power transceivers

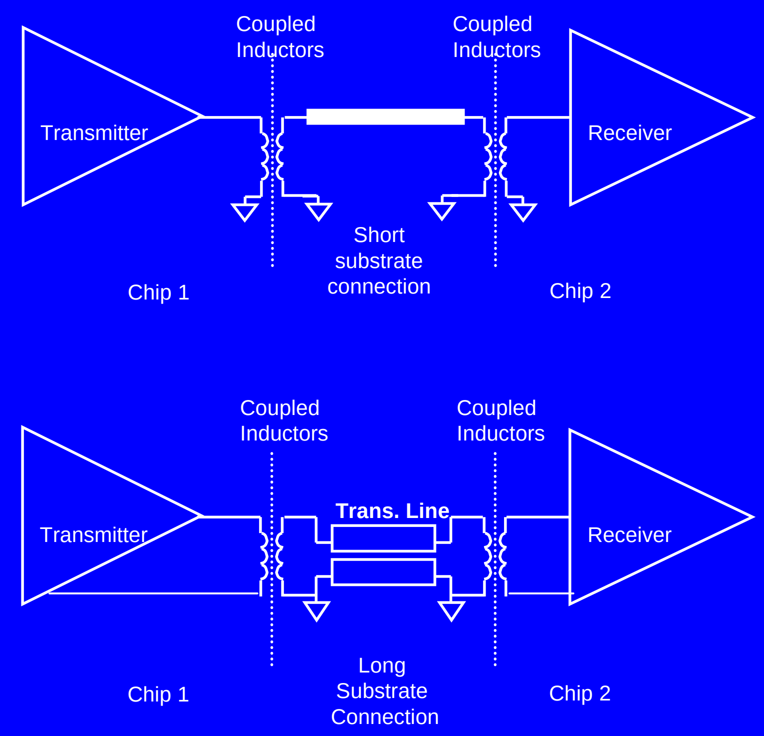


System Models

Capacitive Coupling



Inductive Coupling



Why?

- Need for high density connections
  - Networking : I/O bound (performance)
  - Computing : Vdd/Gnd bound (noise)
  - System level connectivity always underfed
- Cost Considerations
  - Sub-mm pitch connectors/sockets = $$
  - Compliant high density interfaces = Difficult

Achieve end of ITRS roadmap TODAY

Benefits of AC Coupling

- Dense
  - E.g. 600 power/ground + 8,000 signals per sq.cm.
- Manufacturable
  - Little change to manufacturing process
  - **Mechanically Compliant interface**
    - C.f. difficult issue in large arrays of smaller bumps
  - Plate or spiral protected by thin glass
- Broad applications
  - MCMs, packages, sockets, connectors

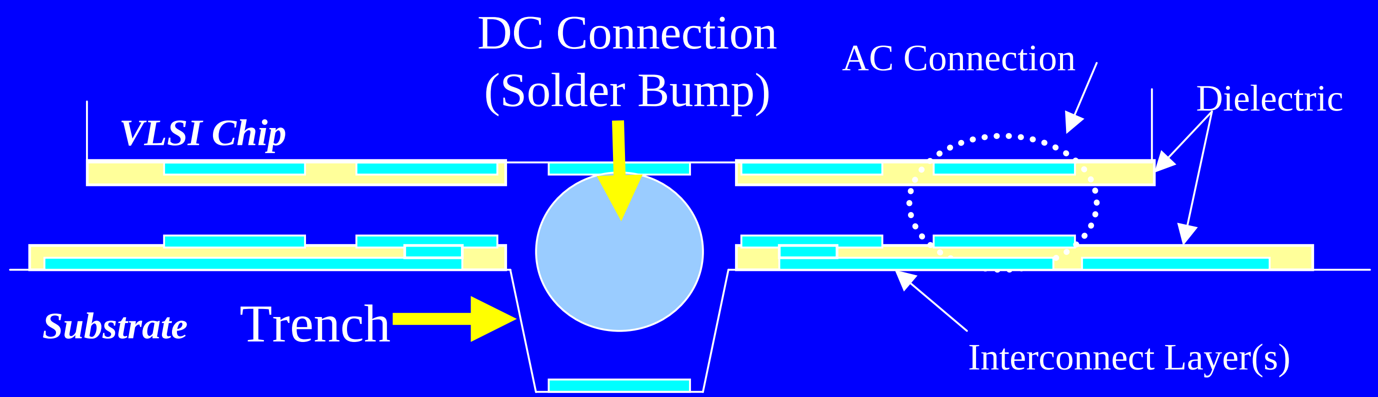
…Benefits

- Low area
  - Minimal ESD requirements
- Good Signal Integrity
  - Large signal swing
  - Series impedance presents wide-band match
  - Impedance matching and termination
  - Reduces SSN

AC Coupled Interconnect

Buried Solder Bump

Overview



- Brings AC pads into controlled proximity
- DC & AC power and ground path
- Solder bumps buried in hole or trench
- Physically performed by
  - Etching; Green Tape punch; Laminate punch

Issues

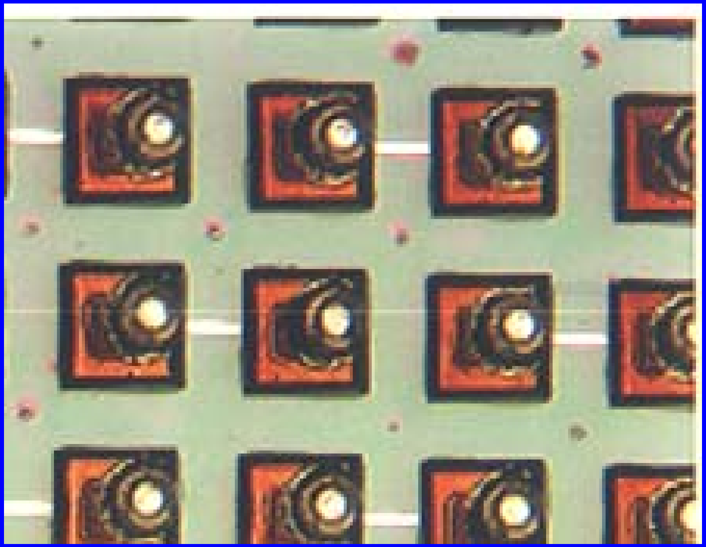
- Coplanarity & gap uniformity
  – More important in capacitive than inductive interconnect
- Alignment
  – Better alignment = improved coupling

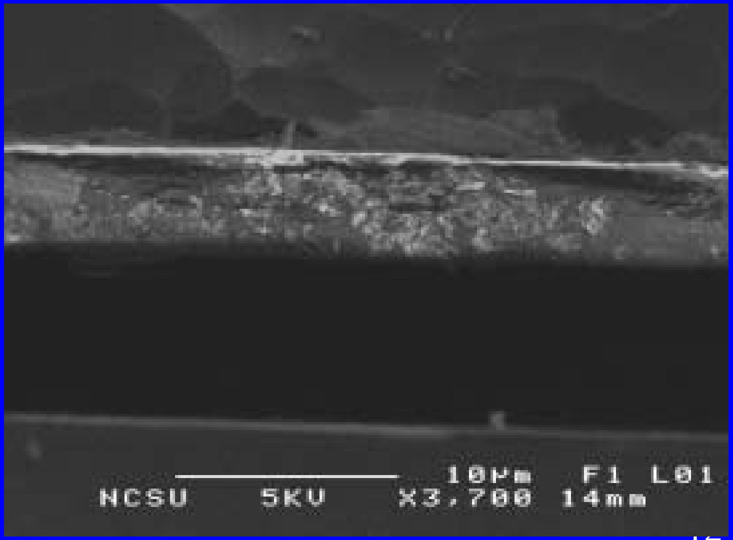
Solved using solder bumps

– Provide precise dimensional control

Physical Demonstration

- Using silicon micromachining and flip-chip solder-bump
  - Gap can be controlled to 1 µm +/- 0.5 µm



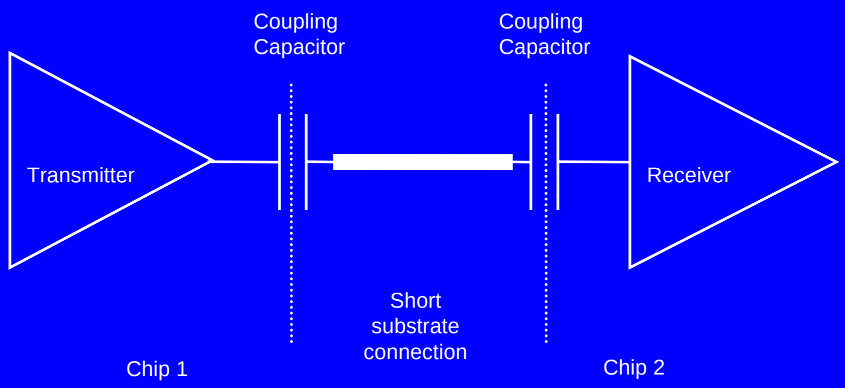


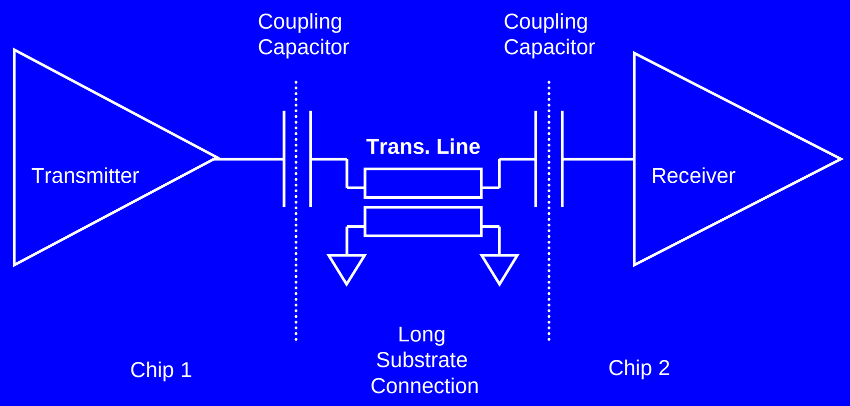
AC Coupled Interconnect

Capacitively Coupled Demonstration

Coupled Capacitor System

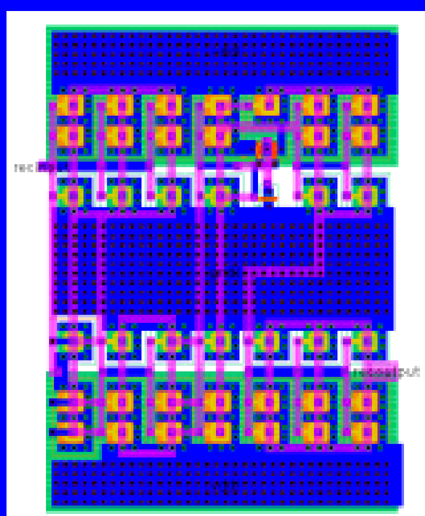
- Can be tuned for impedance match at very high frequencies.
- Voltage mode drivers



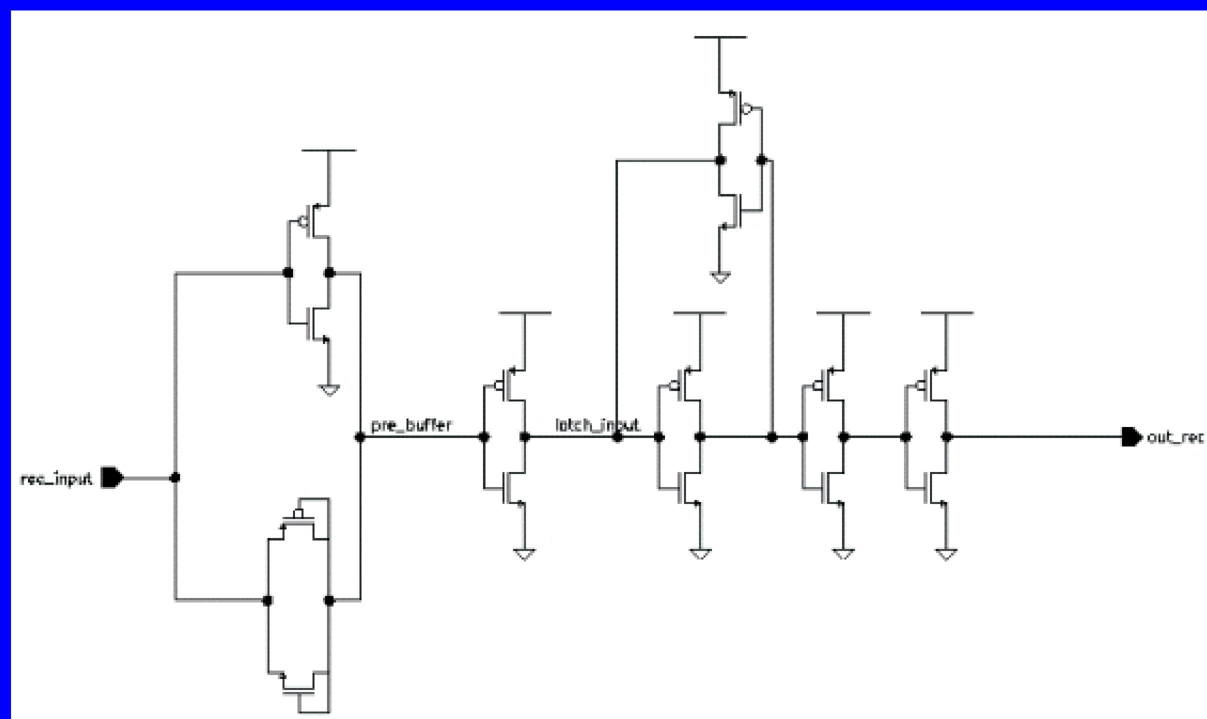


Coupled Capacitor Receiver

- Must be able to recover attenuated NRZ data
  - Want to avoid coding
- Kühn single-ended receiver is capable
  - Diode feedback - Not TX-gate feedback
  - Maintains high gain and high input impedance

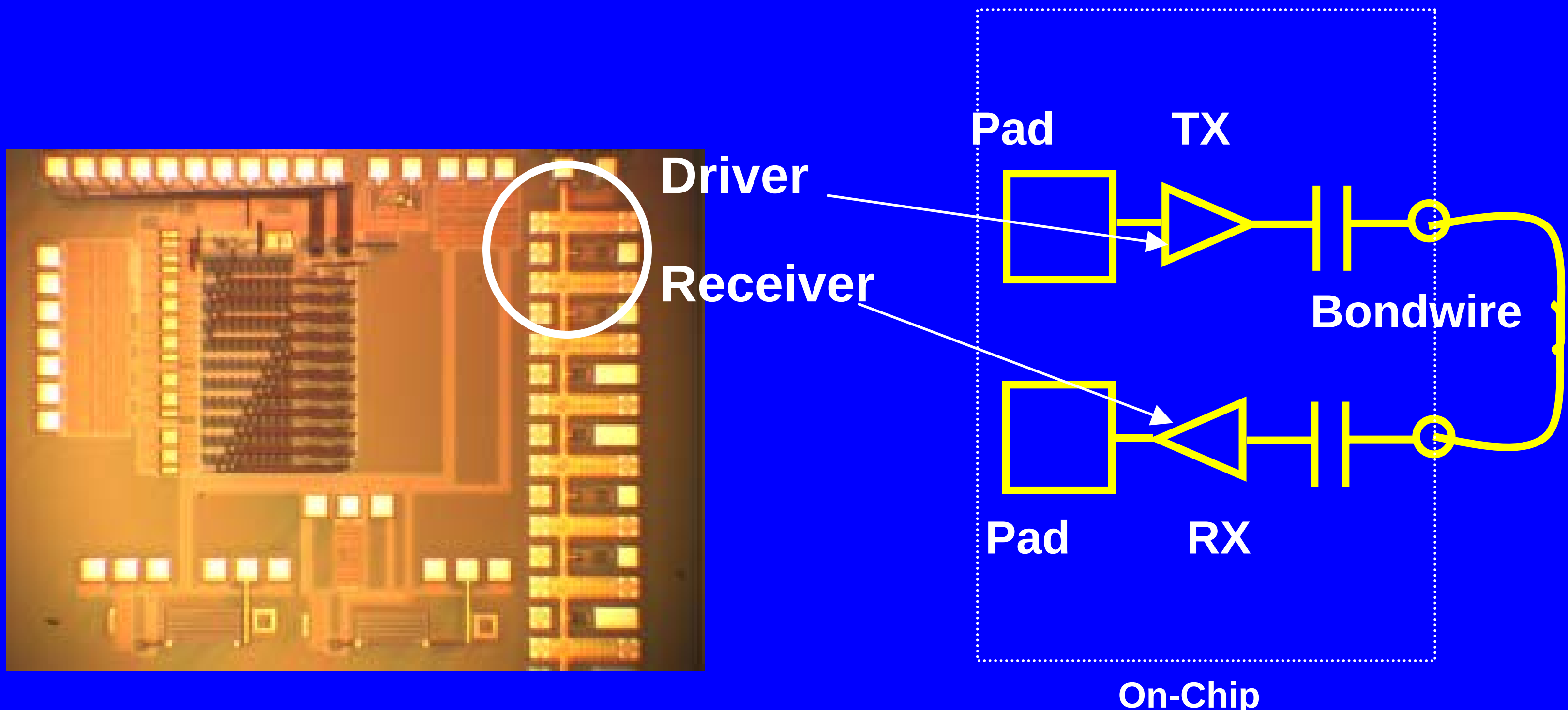


Receiver Layout



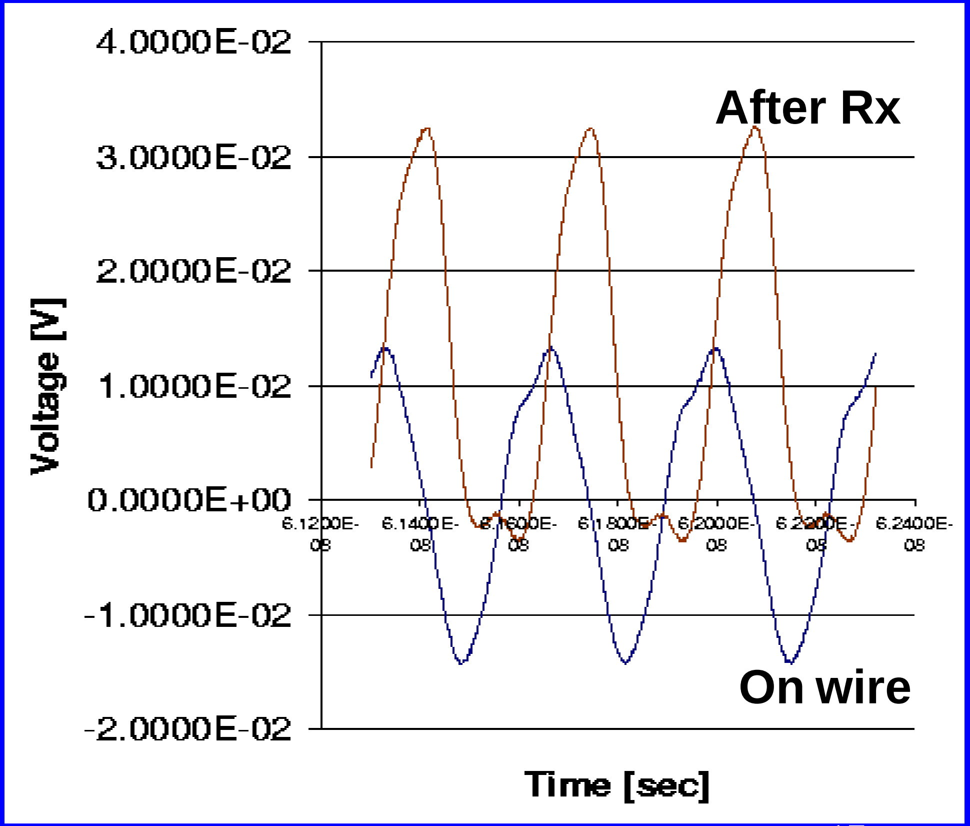
Capacitor Demonstration

- Fabricated through MOSIS in TSMC 0.35 μm technology



Coupled Capactor Results

- Driven up to 3 GHz
  - 0.35 μm CMOS
  - 33 mW
  - 2 V signal
  - 10 mW @ 2 GHz

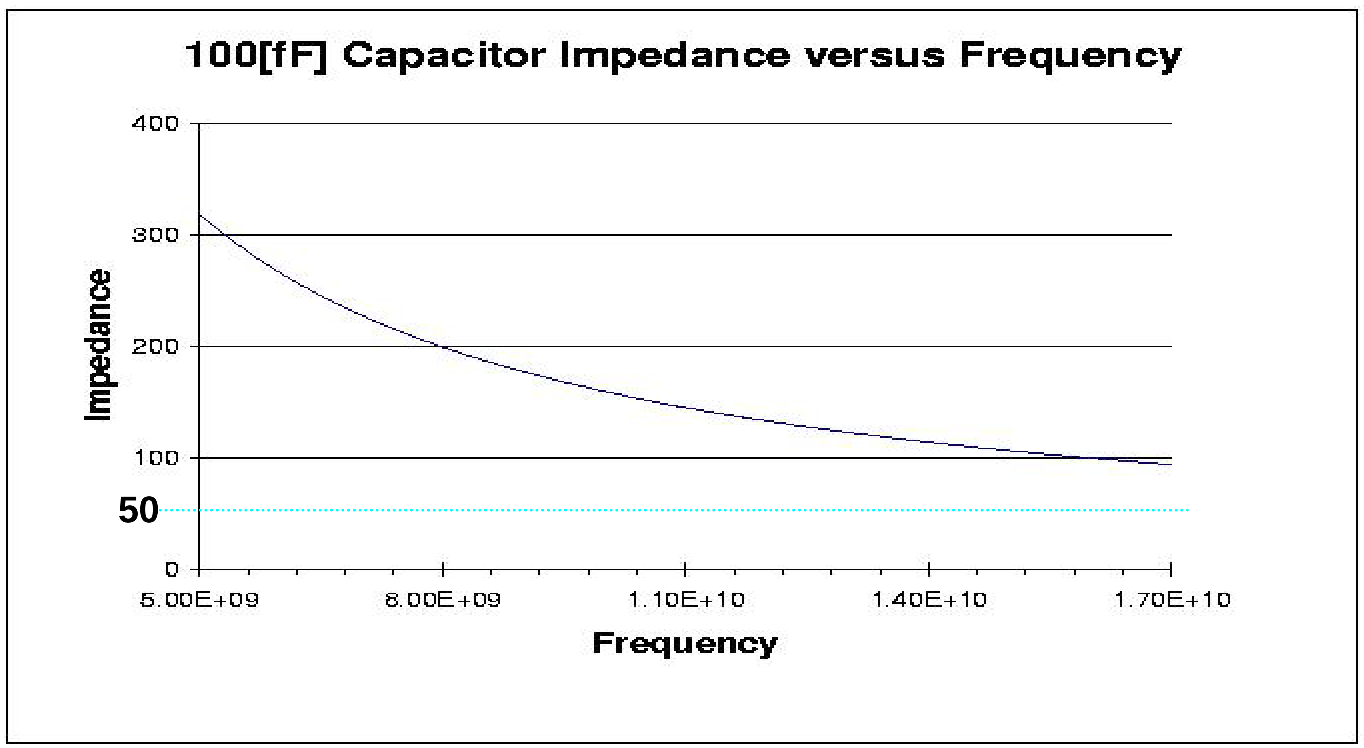


(100:1 7 GHz BW High-Z probe)

Capacitor Impedance Matching

50 Ω match desired in longer lines

- Requires large plates or high K dielectric

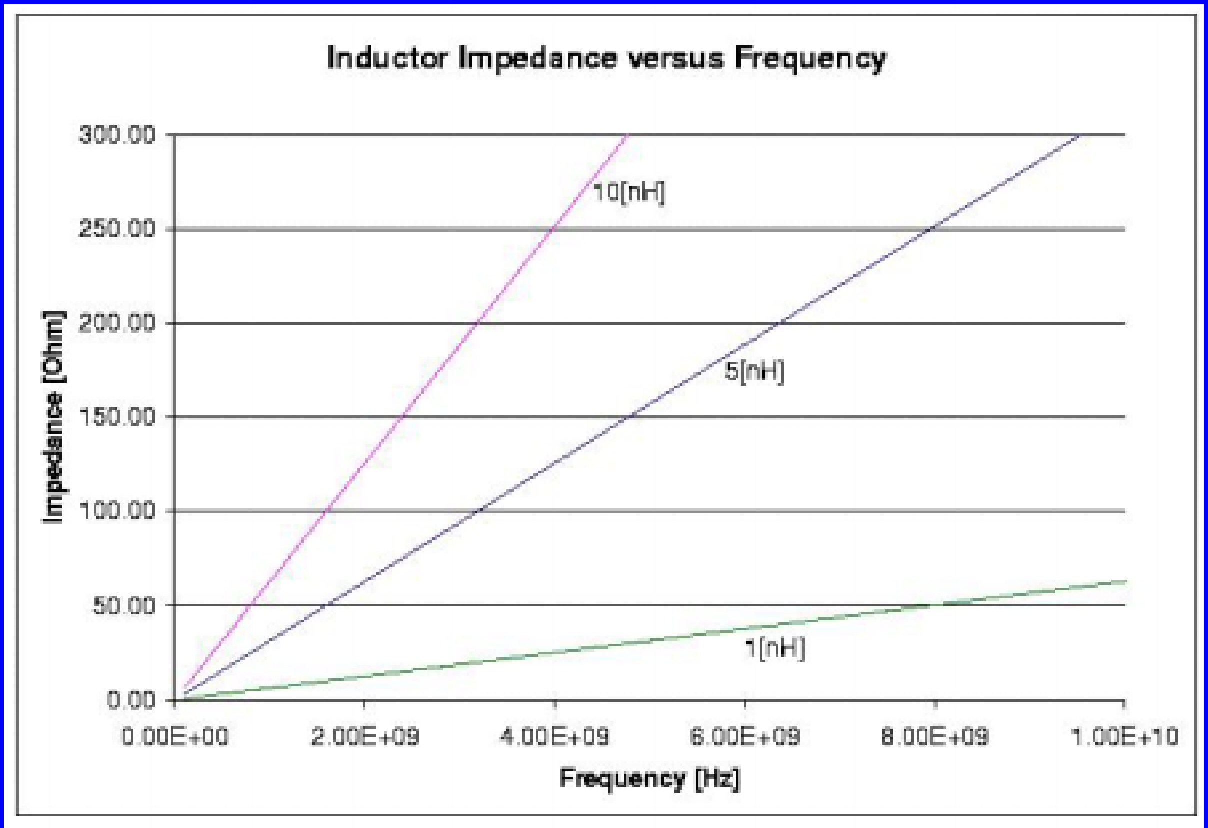


AC Coupled Interconnect

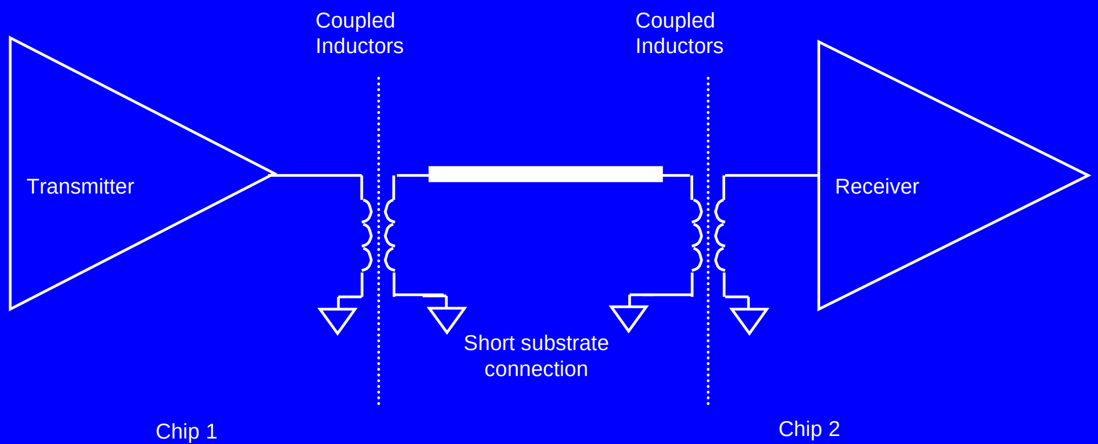
Inductive (Transfomer) Coupling

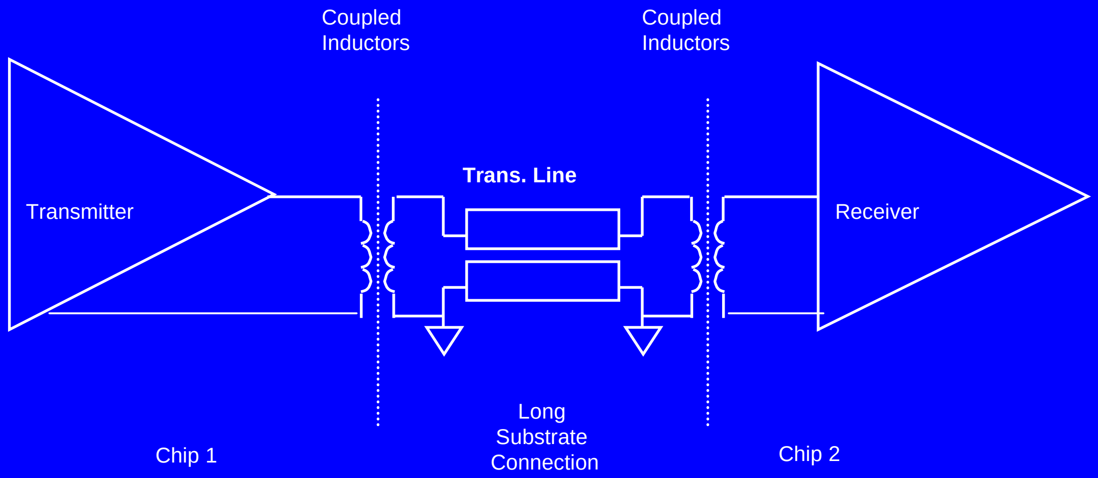
Motivation

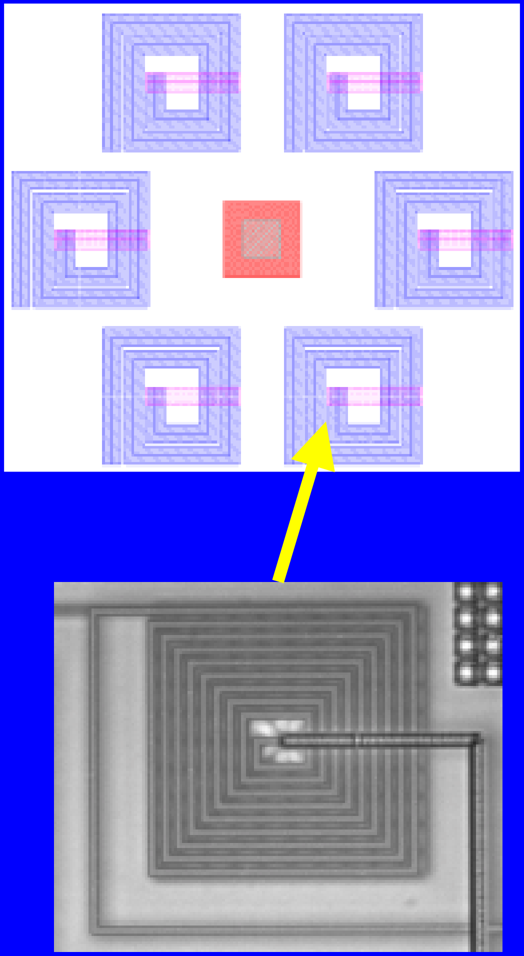
- Easier to provide 50 Ω match
- Reduces need for coplanarity
- Similar density to capacitors



Structures


Coupled Inductors
Coupled Inductors
Transmitter
Receiver
Short substrate connection
Chip 1
Chip 2


Coupled Inductors
Coupled Inductors
Trans. Line
Transmitter
Receiver
Long Substrate Connection
Chip 1
Chip 2

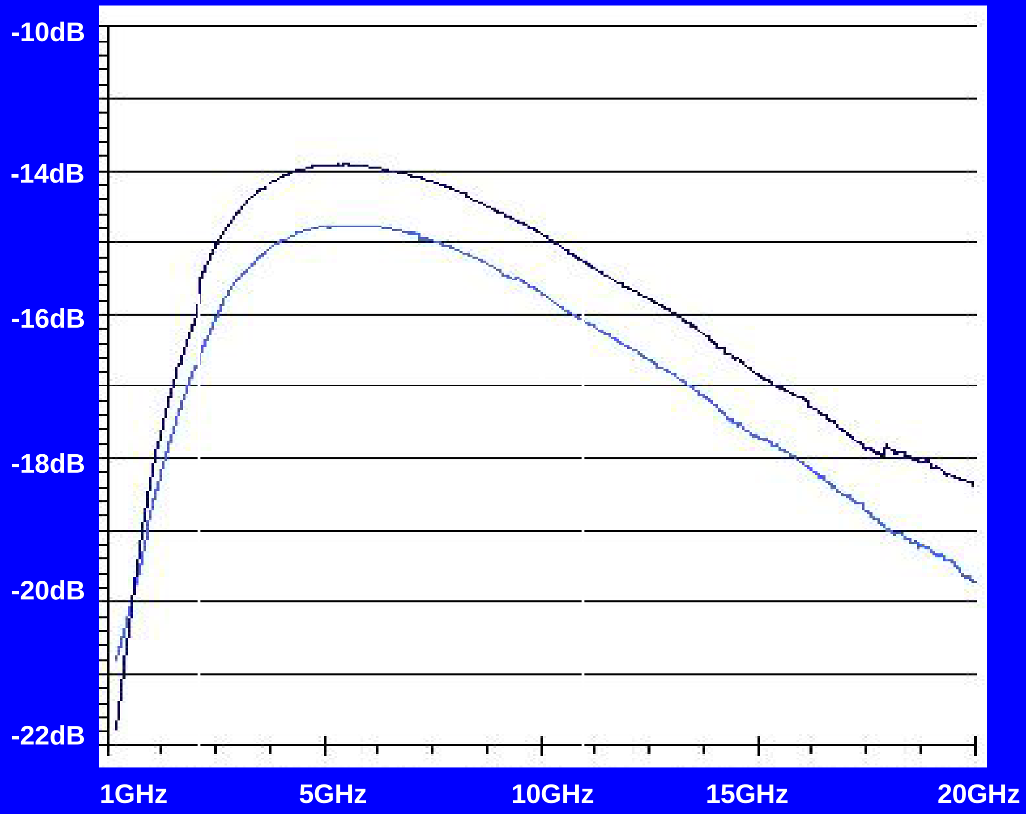


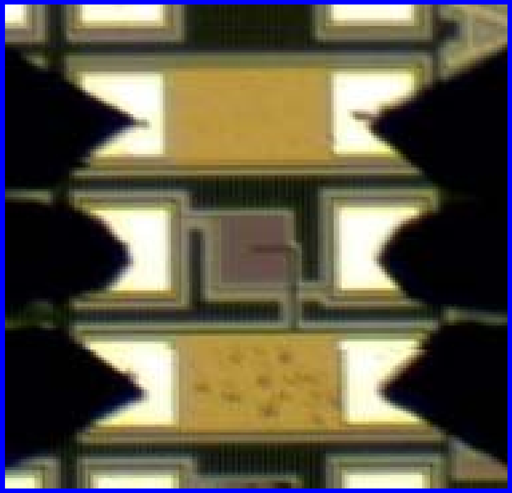
Modeling & Measurement

- On-chip transformers notoriously difficult to model accurately
- Approach:
  - Measure candidate structures
  - Extrapolate models

Coupled Inductor Measurements

TSMC 0.25μm process; 50μm Spiral Inductor; 9 Turns



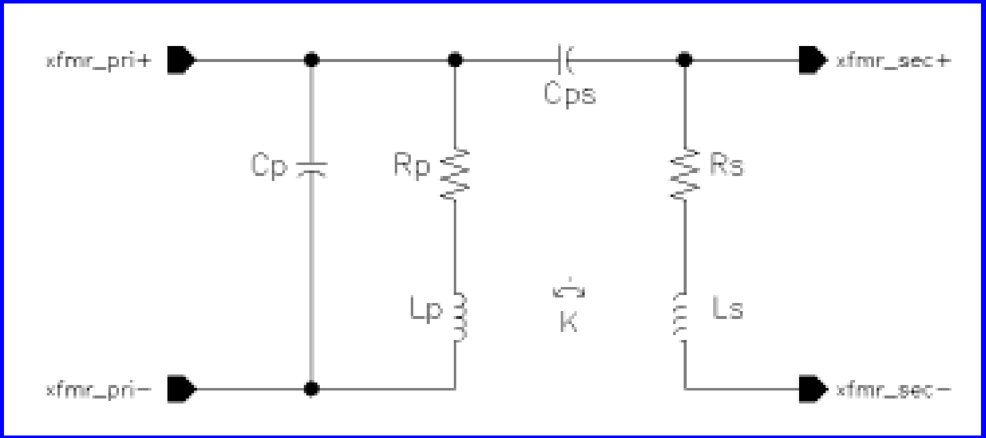


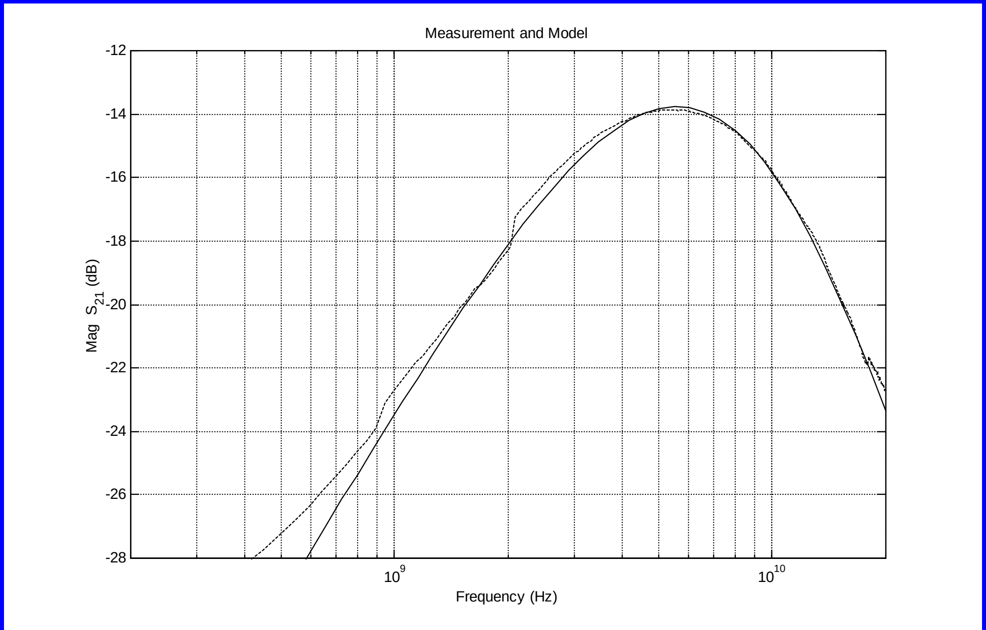
Coupled Inductor Model

- Capacitance and Resistance
  - Calculated from TSMC process parameters
- Inductance calculated from formulas in literature
- Use model to match measurements

Model to Match Measurements

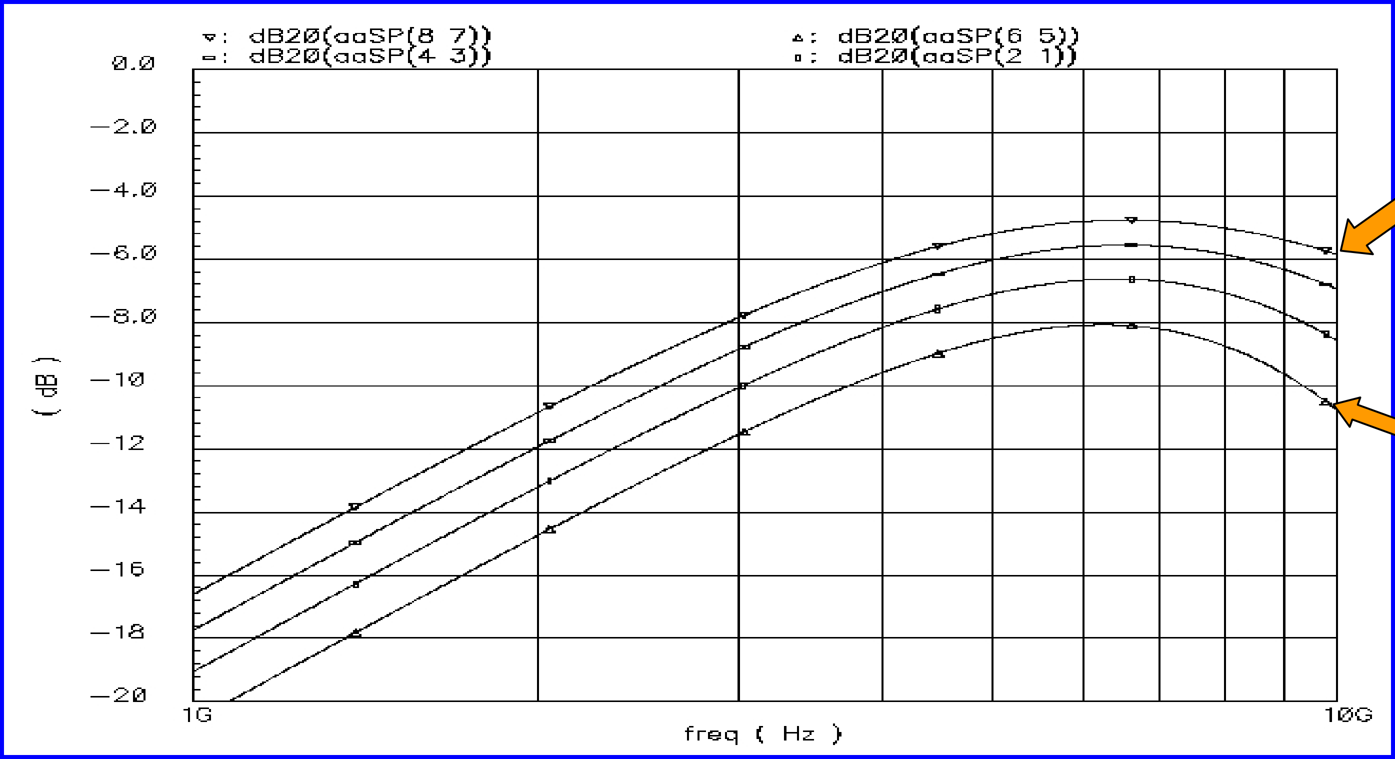
- Lumped model
  - Cp = 180fF
  - Cps = 15fF
  - Rp = 65Ω
  - Rs = 65Ω
  - Lp = 2.8nH
  - Ls = 2.8nH
  - K = 0.5
- **Excellent fit**
- **K low**
  - **Excess loss?**





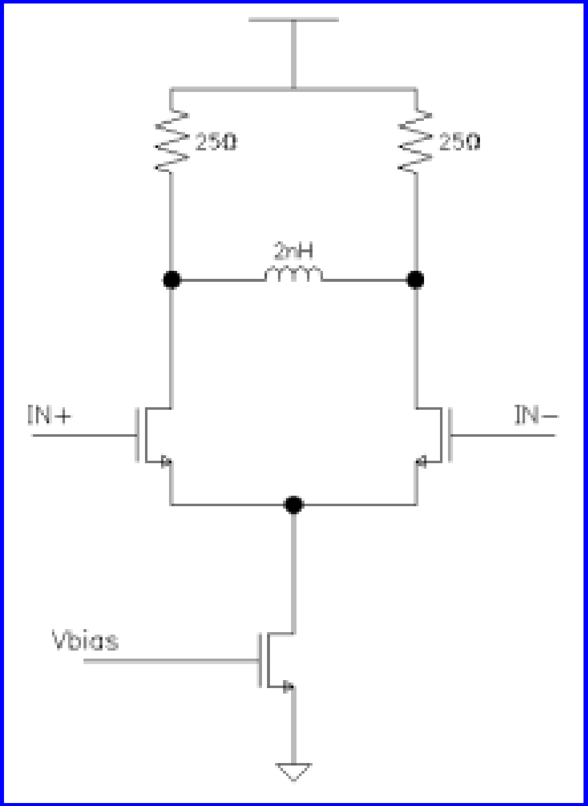
Improved Structure

- Chip inductor : 6 turns
- Package inductor : 3 turns



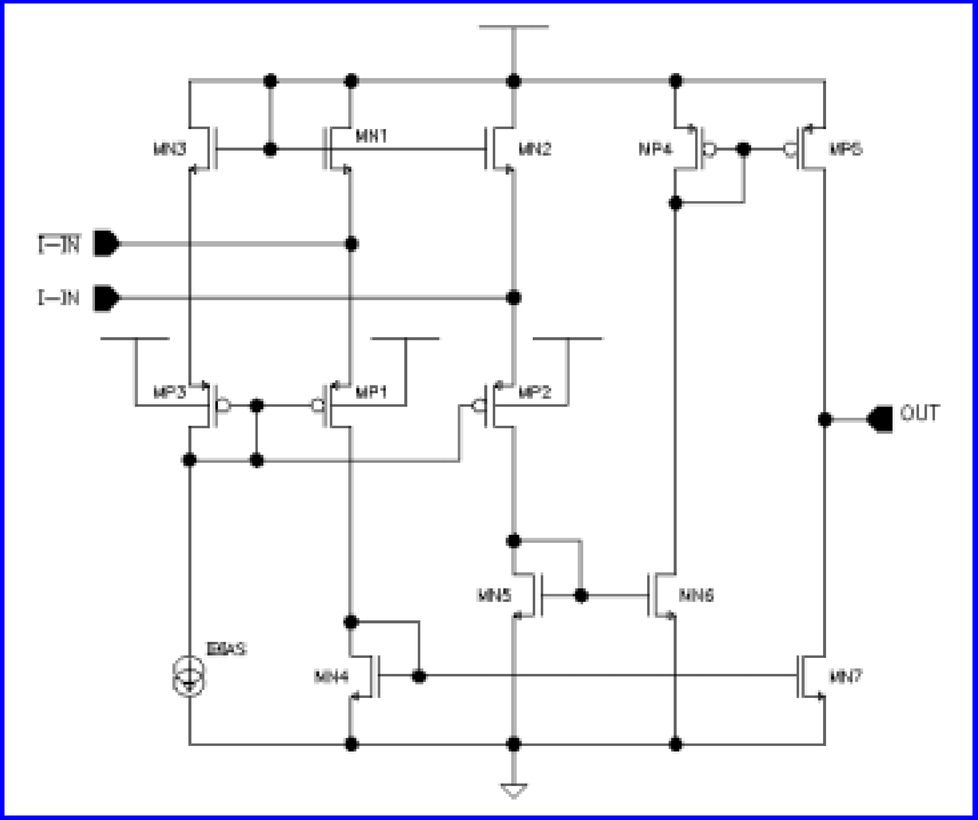
Coupled Inductor Driver

- Simple driver
  - Current steering differential pair
    - Provides flexibility with simple design
    - Low power supply noise
    - Termination provide by on-chip resistors
  - Also investigating H-bridge style driver

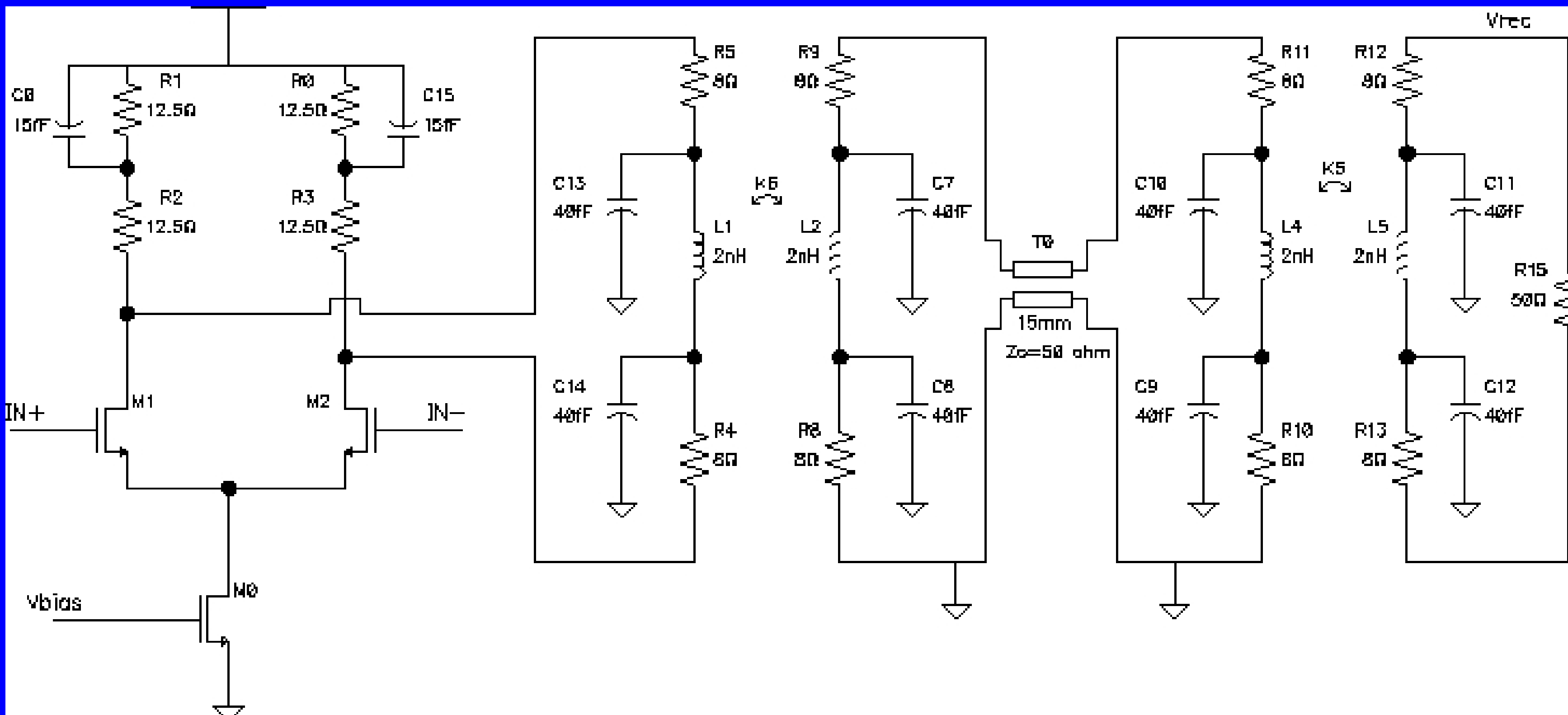


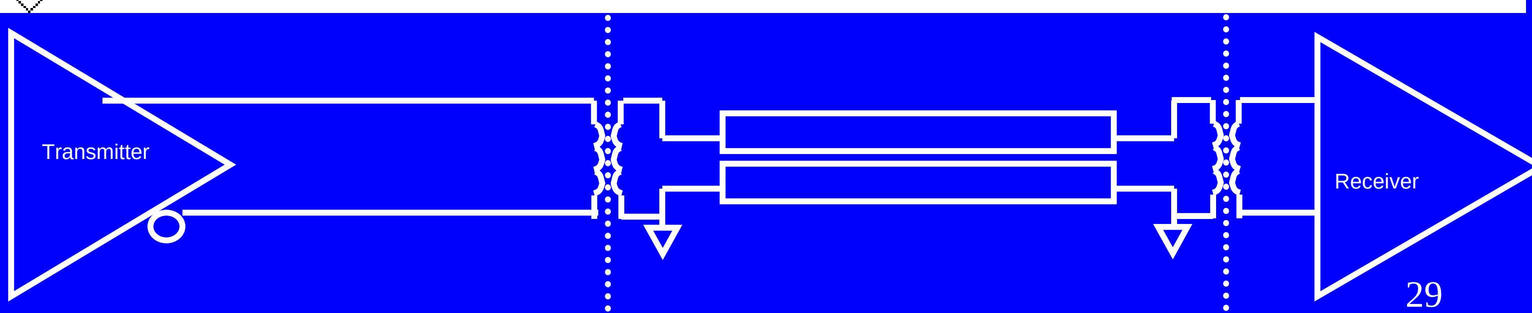
Coupled Inductor Receiver

- Ishibe receiver design for current-mode signaling
  - Constant input impedance



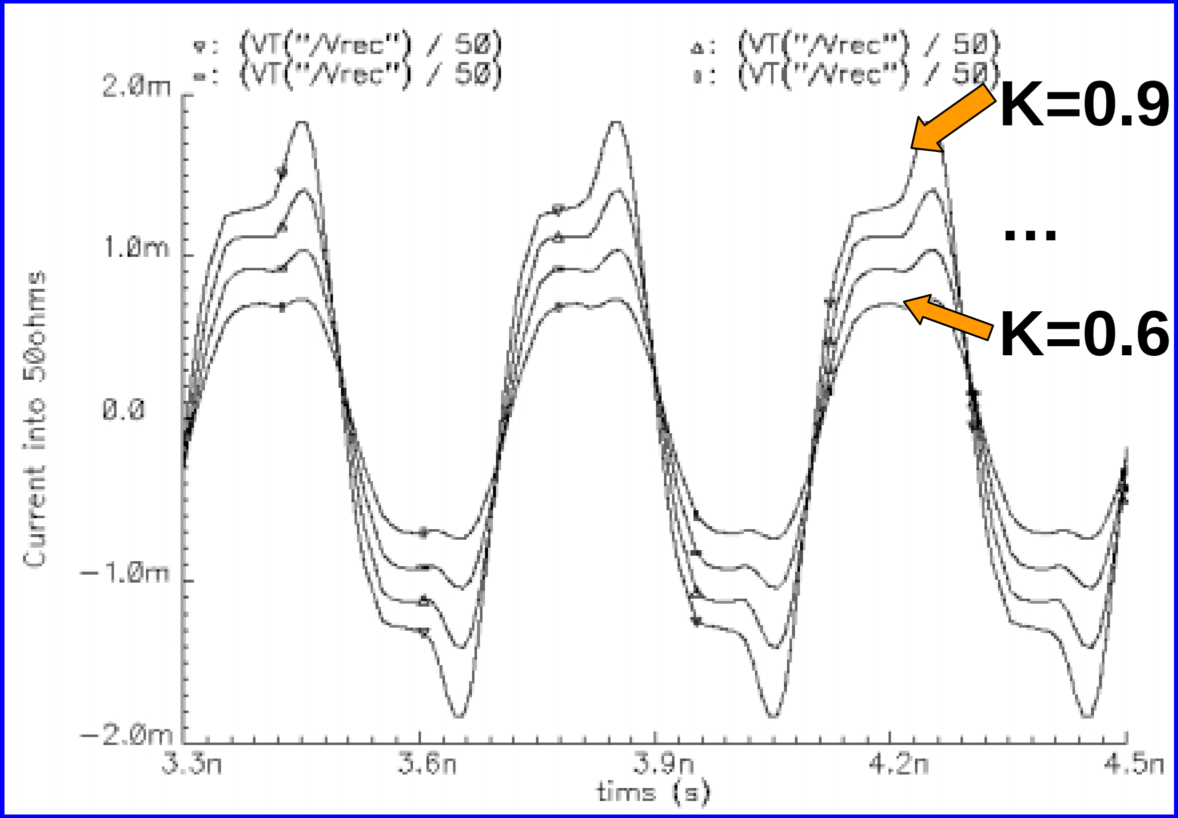
Overall Model





Simulation Results

- 87 mW @ 5 Gbps
- Current @ Receiver input as f(K):



AC Coupled Interconnect

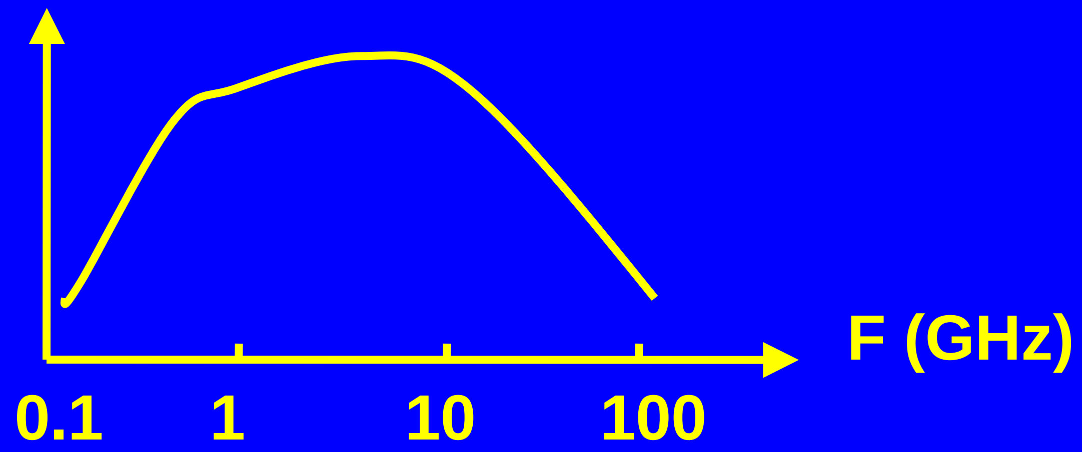
Discussion

FAQs

- Crosstalk?
  - Model results
    - < 1% in capacitive case
    - < 5% in inductive case
- EMI?
  - Not modeled yet
- ESD
  - Reduction expected but how much TBD

…FAQs

- Frequency Characteristics
  - Both provide over a decade of "pass band"



  - Long sequences of 0's and 1's compensated in RX
  - Pass-Band "tunable" by design

Capacitive vs. Inductive

- Capacitive
  - Large plates or high-K dielectric required for longer (>t_r/3 connections)
- Inductive
  - Larger losses
  - Slightly narrower "pass band"
  - More routing impact

Future Work

- Complete demonstration of inductive and capacitive connections
  – Long lines, eye diagram mesurement
- Formulation of design rules
- Demonstration of connector structure

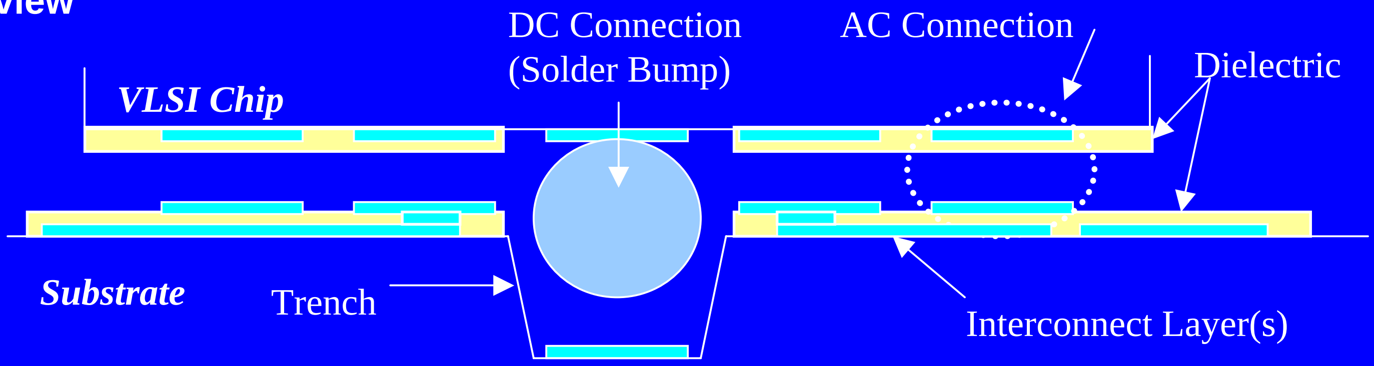
Conclusions

- High density interconnect structure
  - E.g. 600 power/ground + 8,000 signals per sq.cm.
  - Pitch down to 70 μm
- Low-cost interconnect structure
  - Little change to current manufacturing line
  - Compliant physical structure
- Design optimization well under way

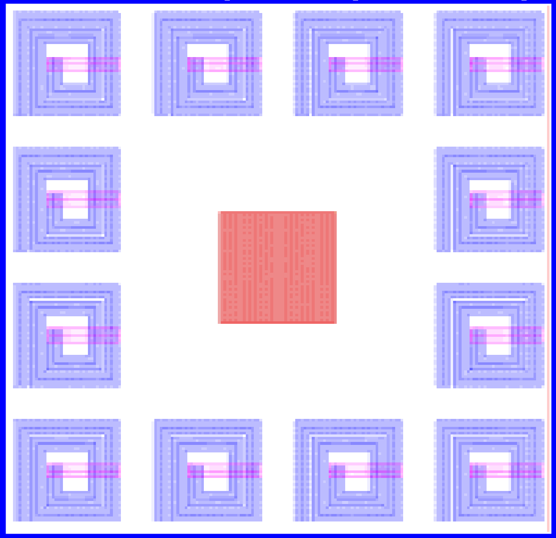
Thankyou

Overview

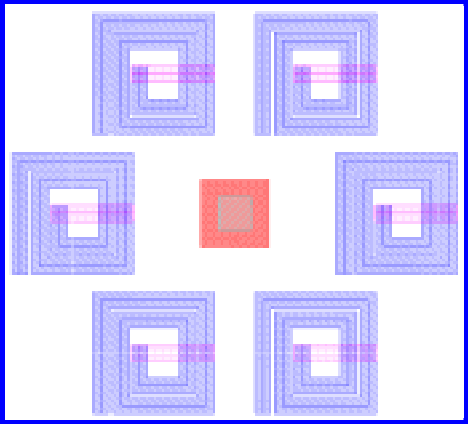
Side view



Unit cell top view (version 1)



Unit cell top view (version 2)



Density Examples

- Future high-performance product 225mm^2
- AC Coupled Interconnect
  - *unit cell version 1 -- non-overlapping square array*
  - 1369 solder bumps: 400 μm pitch → 37 x 37 array
  - 16428 AC pads: 100 μm pitch → 37 x 37 x 12
  - 17797 total connections (subject to wiring constraints)
- AC Coupled Interconnect
  - *unit cell version 2 -- overlapping hexagonal array*
  - 8115 solder bumps: ~400 μm pitch (direct connections on very large pitch, which eases

Physical Structure Issues

- Co-planarity and Alignment
  - Demonstrated (next slide…)
- Metal routing from top to bottom of trench
  - Not currently demonstrated
  - **New process being developed** to address this issue
- Wiring density
  - New process will support multiple routing/interconnect layers

Physical Demonstration (2)

Substrate / Chip Bonding

- Solder bump array permits precise gap control and co-planarity

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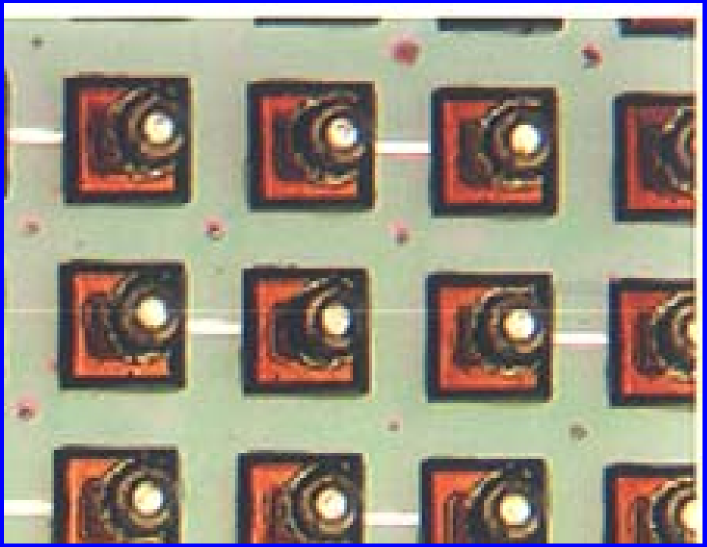
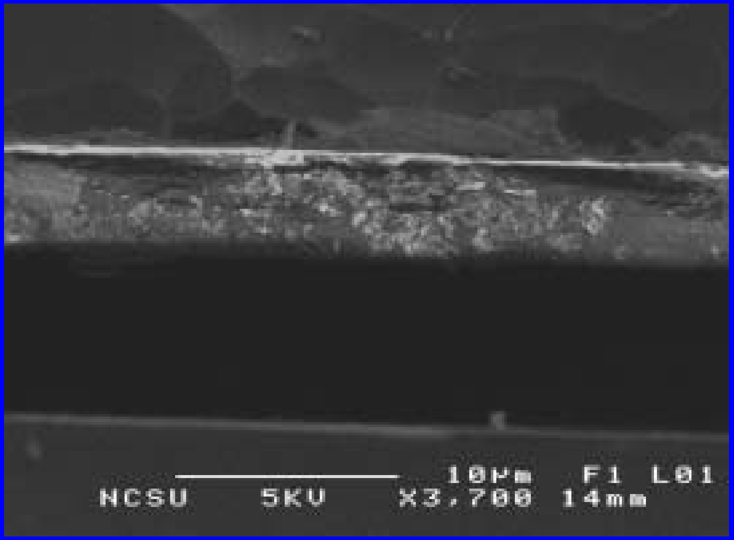


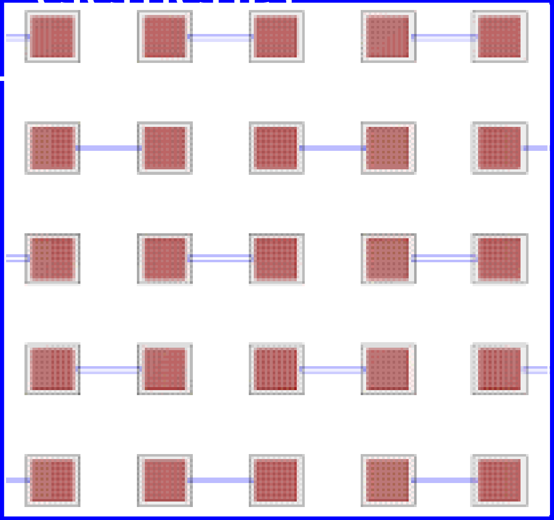
Array After Separation



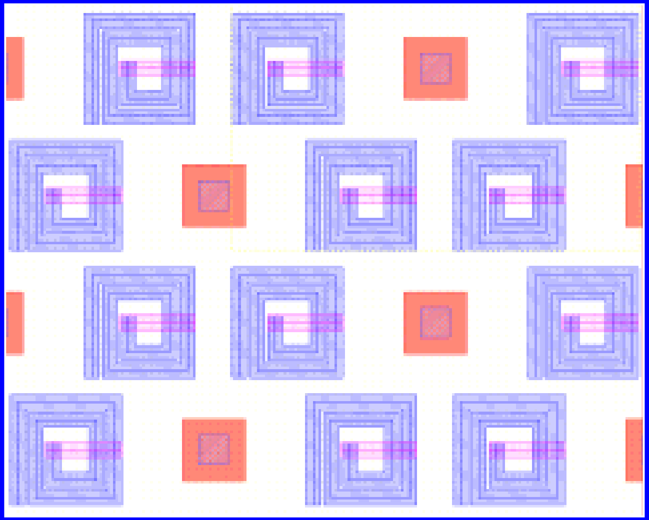
Controllable and Designable Gap

Substrate Process Description

- New 7 layer process
  - Zero level: alignment to crystal lattice
  - 2 metal levels for interconnect and coupling elements
  - er bum



DC test structure



AC test structure

AC Coupled Interconnect

Passive Elements

Passive Element Goals

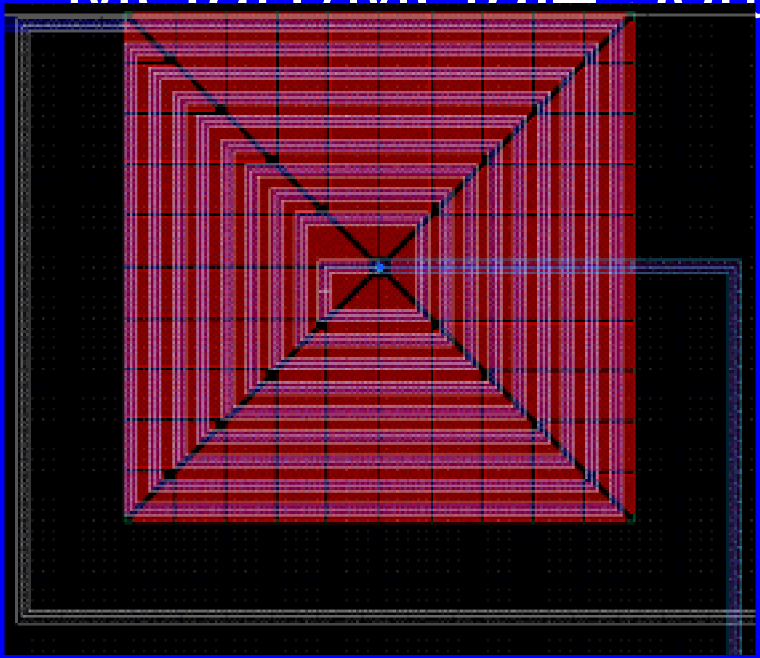
Coupled Inductor System

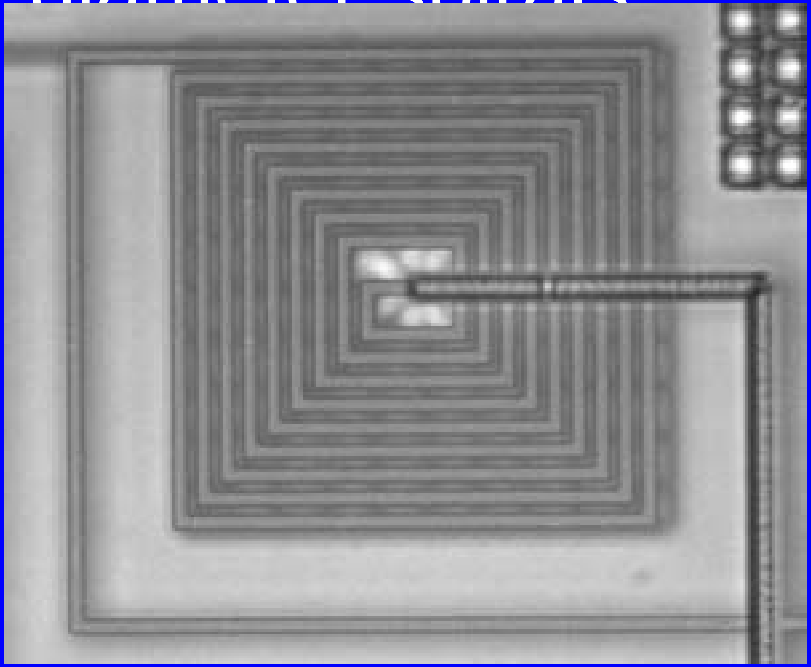
- Develop lumped model
  - match measured data
  - use for new system design
- 50Ohm impedance from transmission line to driver and receiver secondary inductors
- Determine optimal inductor geometry

Physical Demonstration (3)

Coupled Inductor Measurements

- TSMC 0.25μm 5 metal process
- Polysilicon shield
- Metal1/Metal4 50μm diameter spirals





AC Coupled Interconnect

Drivers and Receivers

Driver and Receiver Goals
Coupled Inductor System

- Matched impedance driver and receiver
- Low power dissipation
- 3-6GHz operation
- Current mode operation

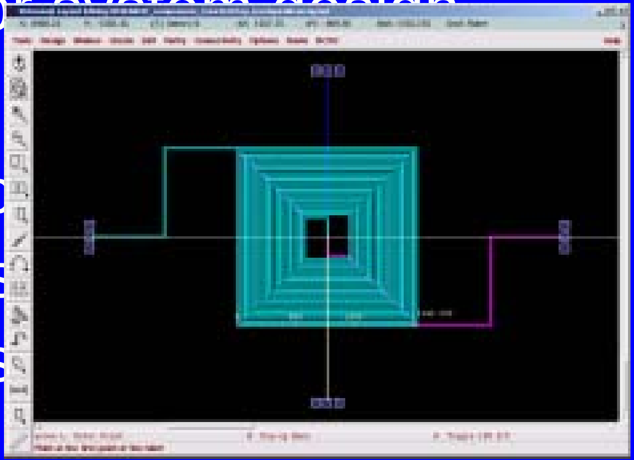
AC Coupled Interconnect

Future Work

Demonstrate feasibility of LC coupled structures

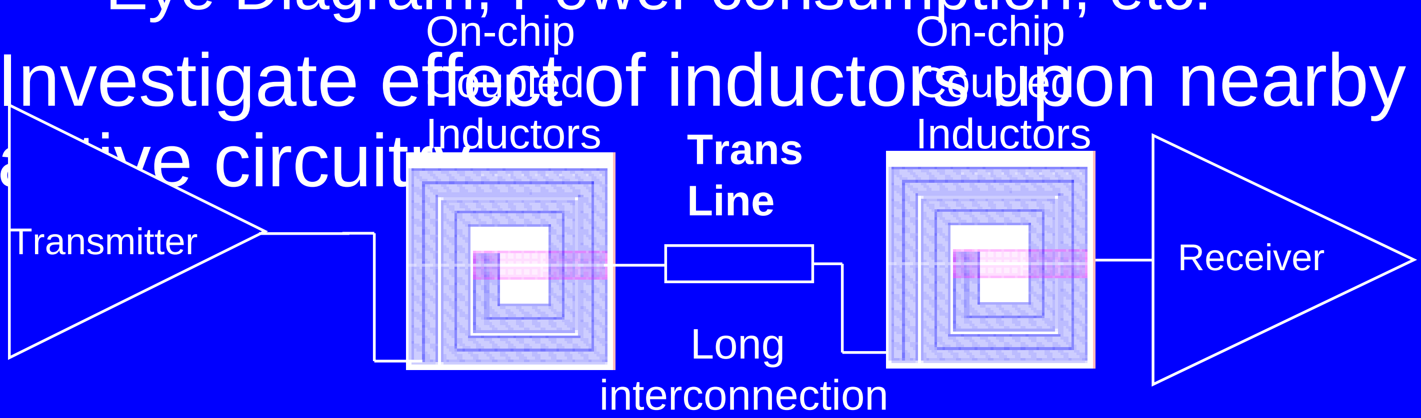
Plan: Future Work

- Complete 2nd generation substrate design and fabrication
- Complete design and fabrication of inductor test structures at NCSU
  - Leads to demonstrated understanding of tradeoffs:
    - turns, turns ratio, crosstalk, wire spacing, wire width, substrate conductivity, parasitics, offset
  - Develop reliable LCRk model fo
- Approach (4” Si wafers)
  - Fabrication in NCSU Clean Roo
  - Test using ERL HF test facilities
  - Account for typical feature sizes in packages



… Plan: Future Work

- Use results from inductor fabrication and improved models to design matched impedance systems
  - On-chip demonstration in MOSIS TSMC 0.25um
- Perform Testing on structure
  - Eye Diagram, Power consumption, etc.
- Investigate effect of inductors upon nearby active circuitry



Open Issues

Have presented several times at member companies.

Recurring Questions

- Underfill & stress relief in general
  - Feasible but not demonstrated
- Different dielectric constants
  - E.g. Use underfill material?
    - Feasible but not demonstrated
- Range of demonstrations
  - Differential, single-sided, through package structures
- Design Rules
  - Optimizing SI in particular circumstances
    - Package and package-chip interaction, ESD, EMI, frequency tuning, etc.
  - Methodology + baseline not yet established
- Sockets and Connectors

Conclusions

- Demonstrated feasibility of buried solder ball concept
- Demonstrated feasibility of capacitively coupled short connections
- Patent filed
- LC-coupled structures permit extension of structure to impedance controlled connection structures
  - Sockets
  - Connectors
- Plans focus on demonstrating feasibility of inductively coupled connections