

# ECE892/Spring - Phase Locked Loop

## ◇◇Course Information ◇◇

‡**Credits:** 3 hours

‡**Text:** *Monolithic Phase-Locked Loops and Clock recovery Circuits*, B. Razavi, IEEE-Press, ISBN 0-7803-1149-3

‡**Time and Place:** Tuesday and Thursday (TBD)

‡**Instructor:** Professor Wentai Liu, Rm. 442 EGRC Building, 5-7347, (wentai@eos.ncsu.edu)

‡**Office Hour:** (TBD)

‡**GRADING:** The course requires a lot of reading about the state-of-art papers. There will not have exam in planning. However each student is expected to make a presentation at least. Also there is lot of matlab work in the first half of the course. In the second half, there is a significant design project based on the given design spec. All works are individual based. *Don't take it if you don't have an urge to become a rare expert in PLL. !!!*

♠ **Policy:** Homeworks should be turn in on time unless preapproval by instructor (10% discount per day)

### ‡**Brief description of the course:**

Design expertise of PLL is one of the most sought talents in the IC industry. It is common that there is at least a PLL incorporating in any non-trivial electronic system. On the other hand, only very few newly graduates know how to design a high performance PLL with CMOS technology. The course is designed to equip our graduate students at NCSU with such a capability.

The students are required to have basic knowledge of time/frequency domain analysis, including transfer function, Laplace and Fourier transform. A knowledge of MATLAB is also advantageous.

The course will cover the operation principle of PLLs, performance parameters, linear and nonlinear characteristics of PLLs, various PLL structures, building block and circuit design for PLLs, applications, and real design examples. Applications will focus on frquency synthesizer, data/clock recovery, clock synchronization.

The course will focus on analog/digital **Phase Locked Loop** and its related issues such as

- mathematical modeling for stability and tracking of PLL
- building blocks for PLL
- circuit designs for PLL
- simulation and macro modeling techniques for PLL
- sources, modelings, and reduction of noise/jitter
- applications of PLL
- PLL in microprocessor design
- techniques for frequency synthesizer
- techniques for data and clock recovery
- challenging design project -  $n$  GHz PLL with  $x$  ps of jitter

The course will divided into the following five phases:

1. Phase-1: PLL fundamental - various digital/analog PLL, mathematical theory of PLL, MATLAB simulation
2. Phase-2: Dealing with Noise/Jitter
3. Phase-3: PLL applications
4. Phase-4: State-of-art papers
5. Phase-5: Experiences sharing with real PLL designers from companies