ECE 720 – ESL & Physical Design

Lecture 21: Repeaters

Spring 2013
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NC State University
Announcements

- Homework #7 Due Monday
Today’s Lecture

- Optimal Repeater Insertion
- Designing with Repeaters
Inverter Delay

- Unit Inverter
  - Minimum length devices, L=50 nm
  - $W_N = W_{\text{unit}}$, $W_P = \text{const} \times W_{\text{unit}}$ (e.g. const=2)
  - same pull-up and pull-down currents
  - approx. equal resistances $R_N = R_P = R_{\text{unit}}$
  - output capacitance $C_{\text{unit}}$
  - approx. equal rise $t_{pLH}$ and fall $t_{pHL}$ delays
- Larger Inverters
  - $s = \text{size}$
  - $W_N = s \times W_{\text{unit}}$, $W_P = s \times \text{const} \times W_{\text{unit}}$
  - $R_N = R_P = R_S = R_{\text{unit}} (W_{\text{unit}}/W_N) = R_{\text{unit}}/s$
  - output (internal) capacitance $C_{\text{int}} = C_{\text{unit}} (W_N/W_{\text{unit}}) = C_{\text{unit}} \times s$
  - Delay = $t_p = 0.69 R_S (C_{\text{int}} + C_L)$

Source: Rabaey
Delay = 0.69 R_s (C_{int} + C_L) = 0.69 R_s C_{int} + 0.69 R_s C_L \\
= 0.69 R_s C_{int} (1 + C_L / C_{int}) \\
= \text{Delay (Internal)} + \text{Delay (Load)}
Delay Formula

\[ \text{Delay} \sim R_S \left( C_{int} + C_L \right) \]

\[ t_p = 0.69 R_S C_{int} \left( 1 + \frac{C_L}{C_{int}} \right) = t_{p0} \left( 1 + \frac{f}{\gamma} \right) \]

- \( C_{int} = \gamma C_{in} \) with \( \gamma \approx 1 \) (1.1 in our process)
- \( f = \frac{C_L}{C_{in}} \) - effective fanout
- \( R_S = R_{unit}/s \)
- \( C_{int} = C_{unit} \cdot s \)
- \( t_{p0} = 0.69 R_{unit} C_{unit} \)

Source: Rabaey
Delay of a Distributed RC Wire

\[ t_p = 0.69 R_S (cL) + 0.38 r c L^2 \]

- \( r \) – resistance per unit length of wire
- \( c \) – capacitance per unit length of wire
- \( L \) – length of wire
Delay with Source & Load Caps

\[ t_p = 0.69R_S(C_S + cL + C_L) + 0.69(rL)C_L + 0.38rcL^2 \]

- \( C_S \) – source (output, internal) capacitance of driver/repeater
- \( C_L \) – load (input) capacitance of driver/repeater
Parameterized for No. of Stages

\[ t_p = m \left( 0.69 \frac{R_d}{s} \left( s \gamma C_d + \frac{cL}{m} + sC_d \right) + 0.69 \frac{rL}{m} (sC_d) + 0.38rc \left( \frac{L}{m} \right)^2 \right) \]

- \( m \) – number of repeaters
- \( R_d \) – output resistance of min. sized driver/repeater
- \( C_d \) – input capacitance of min. sized driver/repeater
- \( s \) – size of each repeater

Optimal Solution

\[ t_p = m \left( 0.69 \frac{R_d}{s} \left( s \gamma C_d + \frac{cL}{m} + s C_d \right) + 0.69 \frac{rL}{m} (s C_d) + 0.38 r c \left( \frac{L}{m} \right)^2 \right) \]

\[ \frac{\partial t_p}{\partial m} = \frac{\partial t_p}{\partial s} = 0 \]

\[ m_{opt} = L \sqrt{\frac{0.38 r c}{0.69 R_d C_d (\gamma + 1)}} = \sqrt{\frac{t_{p\text{wire(unbuffered)}}}{t_{p1}}} \]

\[ s_{opt} = \sqrt{\frac{R_d c}{r C_d}} \]

- \( t_{p1} = t_{p0}(1 + 1/\gamma) = 0.69 \ R_d \ C_d \ (\gamma + 1) \)
  
  » delay of a fan-out 1 inverter

- Remember that \( t_{p0} = 0.69 \ R_d \ C_d \gamma \)
Critical Wire Length

\[ L_{\text{crit}} = \frac{L}{m_{\text{opt}}} = \sqrt{\frac{t_{p1}}{0.38rc}} \]

\[ t_{p, \text{min}} = (1.38 + 1.02\sqrt{1 + \gamma})L\sqrt{R_d C_d rc} \]

\[ t_{p, \text{crit}} = \frac{t_{p, \text{min}}}{m_{\text{opt}}} = 2 \left( 1 + \sqrt{\frac{0.69}{0.38(1 + \gamma)}} \right) t_{p1} \]

- \( L_{\text{crit}} \) = optimal length of wire-segments between repeaters for a given technology and interconnect layer
Questions

- Which cases does this formulation optimize?

- How would the solution change for other cases?

- How would you implement this in a practical design?
Today’s Lecture

- Optimal Repeater Insertion
- Designing with Repeaters
Encounter Repeater Insertion

- repeater.rule file needed: For each cell, need to specify the maximum wire length (in microns) of the wire and maximum net capacitance (in pF) that it can drive
- How would you calculate these values?

```
#cell INV_X1 uses template Timing_X1
SetBufferDrivingStrength INV_X1 50 0.012800

#cell INV_X2 uses template Timing_X2
SetBufferDrivingStrength INV_X2 101 0.025600

#cell INV_X4 uses template Timing_X4
SetBufferDrivingStrength INV_X4 203 0.051200

#cell INV_X8 uses template Timing_X8
SetBufferDrivingStrength INV_X8 407 0.102400
```
Estimations of $L_{\text{max}}$

Fig. 6. $L_{\text{max}}$ becomes less than twice the chip-side length past 130-nm for minimum-pitch fat wiring. Wiresizing allows $L_{\text{max}}$ to exceed $2 \times D_e$ at all technology nodes.

- Source: Sylvester & Keutzer 2000
New Global Wiring Paradigm

- Source: Sylvester & Keutzer 2000
- 50nm microprocessor example
## Technology Comparison

<table>
<thead>
<tr>
<th></th>
<th>2007 (45 nm)</th>
<th>2016 (16 nm)</th>
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<th>2016 (16 nm)</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>capacitance (fF/\mu m)</td>
<td>resistance (\Omega/\mu m)</td>
<td>capacitance (fF/\mu m)</td>
<td>resistance (\Omega/\mu m)</td>
</tr>
<tr>
<td>M1</td>
<td>0.19</td>
<td>0.16</td>
<td>4.7</td>
<td>67</td>
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<tr>
<td>Intermediate</td>
<td>0.18</td>
<td>0.13</td>
<td>4.1</td>
<td>70</td>
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<td>Global</td>
<td>0.2</td>
<td>0.15</td>
<td>1.1</td>
<td>17</td>
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</tbody>
</table>

- Numbers derived from the 2007 ITRS
Technology Comparison

- $L_{\text{crit}}$ is dropping rapidly, global interconnect delay rising
- Number of repeaters for minimum delay will rise exponentially (could overtake logic gates)
- optimum delay below calculated using slide 10 equations

<table>
<thead>
<tr>
<th></th>
<th>2007 (45 nm)</th>
<th>2016 (16 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_d$ (Ω-µm)</td>
<td>901</td>
<td>296</td>
</tr>
<tr>
<td>$C_d$ (fF/µm)</td>
<td>0.47</td>
<td>0.33</td>
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<tr>
<td>$\gamma$</td>
<td>1.51</td>
<td>1.55</td>
</tr>
<tr>
<td>$t_{p1}$ (fs)</td>
<td>734</td>
<td>170</td>
</tr>
<tr>
<td>$L_{\text{crit}}$ (µm)</td>
<td>92</td>
<td>13</td>
</tr>
<tr>
<td>$W_{\text{opt}}$ (µm)</td>
<td>18</td>
<td>2.9</td>
</tr>
<tr>
<td>opt. delay (ps/mm)</td>
<td>29</td>
<td>47</td>
</tr>
</tbody>
</table>