ECE 747
Digital Signal Processing Architecture

SoC Lecture – Working with Buses & Interconnects

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Today’s Lecture

- Introduction
  - AMBA Peripheral Bus (APB)
  - AMBA High-Performance Bus (AHB)
  - AMBA Extensible Interconnect (AXI)

Why do we care?

- What is a Bus?
- What is an Interconnect?
- Why do we use them?

Our Question

- Which bus or interconnect should we use?

The answer depends on the following:
  » What IP blocks do we have and what do they work with?
  » How many ports do we need?
  » What kind of overhead can we permit?
    - Throughput
    - Area
    - Power
Bus & Interconnect Standards

- AMBA from ARM
- Wishbone from OpenCores.org
- CoreConnect from IBM
- Sonics “Silicon Backplane”

We’ll focus on AMBA in this class, because it’s the one our simulator models.

AMBA Introduction

- Advanced Microcontroller Bus Architecture (AMBA), created by ARM as an interface for their microprocessors.
- Easy to obtain documentation (free download) and can be used without royalties.
- Very common in commercial SoC’s (e.g. Qualcomm Multimedia Cellphone SoC)
- AMBA 2.0 released in 1999, includes APB and AHB
- AMBA 3.0 released in 2003, includes AXI

AMBA 2.0 System-Level View

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**APB Introduction**

- Low overhead – only 4 control signals
- Only one master is allowed
- Three states: IDLE, SETUP, and ENABLE
- Slave is non-responsive: Transfer always takes 2 cycles
  » Makes timing easy to design: data is always latched between the two cycles

**APB Read Transaction**

- Transaction takes 2 cycles: SETUP & ENABLE

**APB Write Transaction**

**APB Performance**

- If AHB is “high performance” than APB must be “low performance”. What does that mean?
- If we were to connect an SDRAM as an APB slave from the previous lecture, what would our minimum bus clock period be?
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AHB Introduction

- Larger overhead – ~27 control signals
- Up to 15 masters allowed
- Split Transaction phases: Address, Data (Pipeliend)
- HREADY signal allows insertion of wait-states

AHB Architecture

- Central MUX is used, rather than a bus
- Achieves smaller delays than a single wire with tri-state buffers

Source: AMBA Specification, Rev. 2.0

AHB Split-Transaction Bus

- Address preceeds data by one cycle
- Mimics SDRAM operation, achieves greater data bandwidth

Source: AMBA Specification, Rev. 2.0
Multiple Transactions w/ AHB

- Addresses are pipelined to improve memory efficiency
- HREADY from slave allows insertion of wait states

Source: AMBA Specification, Rev. 2.0

AHB Burst Operation

- Bursts with lengths up to 32 are allowed
- What would happen if an incrementing burst read to a DRAM row boundary?

AHB Access Grant Mechanism

- Bus arbitration takes extra cycles

Source: AMBA Specification, Rev. 2.0

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AXI Introduction

- Larger overhead – ~77 control signals
- Up to 16 masters allowed
- 5 separate channels for address, data, and responses
- Not so much of an interconnect specification as a protocol (interconnect architecture is left unspecified)

Multi-Channel Support

- Address, Data, and Response split between channels, rather than phases
- Allows simultaneous reads and writes

AXI Read Transactions

- Up to 16 transactions can be queued at once

Multi-Layer Connectivity

- PL300 Interconnect is implemented as a crossbar:
- Multiple masters can talk to multiple slaves simultaneously
# Comparison of AMBA Bus Types

<table>
<thead>
<tr>
<th></th>
<th>APB</th>
<th>AHB</th>
<th>AXI / PL300</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processors</td>
<td>all</td>
<td>ARM7,9,10</td>
<td>ARM11</td>
</tr>
<tr>
<td>Control Signals</td>
<td>4</td>
<td>27</td>
<td>77</td>
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<tr>
<td>No. of Masters</td>
<td>1</td>
<td>1-15</td>
<td>1-16</td>
</tr>
<tr>
<td>No. of Slaves</td>
<td>1-15</td>
<td>1-15</td>
<td>1-16</td>
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<td>Interconnect Type</td>
<td>Central MUX?</td>
<td>Central MUX</td>
<td>Crossbar w/ 5 channels</td>
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<tr>
<td>Phases</td>
<td>Setup, Enable</td>
<td>Bus request, Address, Data</td>
<td>Address, Data, Response</td>
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<tr>
<td>Xact. Depth</td>
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<td>2</td>
<td>16</td>
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<tr>
<td>Burst Lengths</td>
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<td>1-16</td>
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<tr>
<td>Simultaneous Read &amp; Write</td>
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<td>no</td>
<td>yes</td>
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