

# LAB MODULE 4 OF 4: OTFT

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## ***Fabrication and Characterization of an Organic Thin Film Transistor***

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### **Abstract**

This lab experiment is designed to help you understand the construction and operation of an **Organic Thin Film Transistor** (OTFT). You will learn the importance of the electrodes, organic layers, and the other infrastructure comprising an OTFT in the process of fabricating and characterizing your own. Starting from the conductive, transparent and interdigitated indium tin oxide (ITO) source and drain electrodes, you will apply an organic layer, P3HT (poly(3-hexylthiophene)), and an insulating layer, PVP (polyvinyl propylene). You will then create a gate structure containing a liquid metal (gallium-indium eutectic) and finalize the assembly using optical adhesive. Finally, you will characterize your OTFT by measuring current vs. voltage data, determining the turn-on voltage, and analyzing the various operation regimes.

<u>Part 1</u>	<u>Part 2</u>	<u>Part 3</u>
Semiconducting and Insulating Layers	Creating the Gate Electrode and the OTFT	Device Characterization

### **Write-up Instructions**

Your lab report (Lab Notebook) will minimally consist of the following *for each part*:

- A. Statement of experimental objective
- B. Sketches of experimental setup
- C. Record of all measurements
- D. All requested calculations

The following lab procedure will indicate specifically what to include and where. The purpose of this style of write-up is to force you to keep a technical record of your experiments in the way that many engineers and scientists are required to do (in industry and universities). The lab director(s) will provide you with blank technical notebook sheets in the lab (also available on the website). You are expected to follow the lab notebook guidelines introduced by the lab director(s) (also see the Appendix), and your lab grade will depend both on your experimental procedure and on how well you follow these guidelines. Note that the same pages you use during the lab experiment should also be the ones you complete at home and hand-in as your write-up — do not rewrite them.

## A Brief History of Organic Thin Film Transistors (OTFT)

Identified in the 1950s, research related to organic semiconductors remained confidential until the late 1980s—about the time organic LEDs (OLED) and organic photovoltaics (OPV) were becoming hot research topics. Using a thin film transistor (TFT) architecture, organic materials (polymers, oligomers), hybrid materials (organic-inorganic composites), and small molecules have been employed in the development of TFTs. This same architecture had proved viable when hydrogenated amorphous silicon (a-Si:H) was used as the semiconducting material. Even today, a-Si:H is used for the transistor backplanes in liquid crystal displays (LCD) and OLED displays [1].

Originally, charge carrier mobility was the parameter of focus since it was a key factor limiting any performance breakthrough. As better materials and device structures were discovered, researchers showed that OTFT performance could rival that of a-Si:H TFTs. The development over time of charge carrier mobility is shown in Fig. 1. Note that in a period of fewer than 15 years, mobility of organic semiconductors has improved by five orders of magnitude, rivaling the performance of traditional inorganic devices.

Over the past few decades, several academic and industrial groups have undertaken OTFT research and development, searching for better photoresists, electrode materials and insulators in focused and broad efforts to improve overall semiconducting properties, to bring processing difficulty and constraints to a minimum and to open new application pathways such as large-area printing on common and accessible materials. Current excitement surrounding OTFTs is driven by the ability to print transistor arrays on flexible backplanes for electronic displays, including e-paper, LCDs and OLED displays.

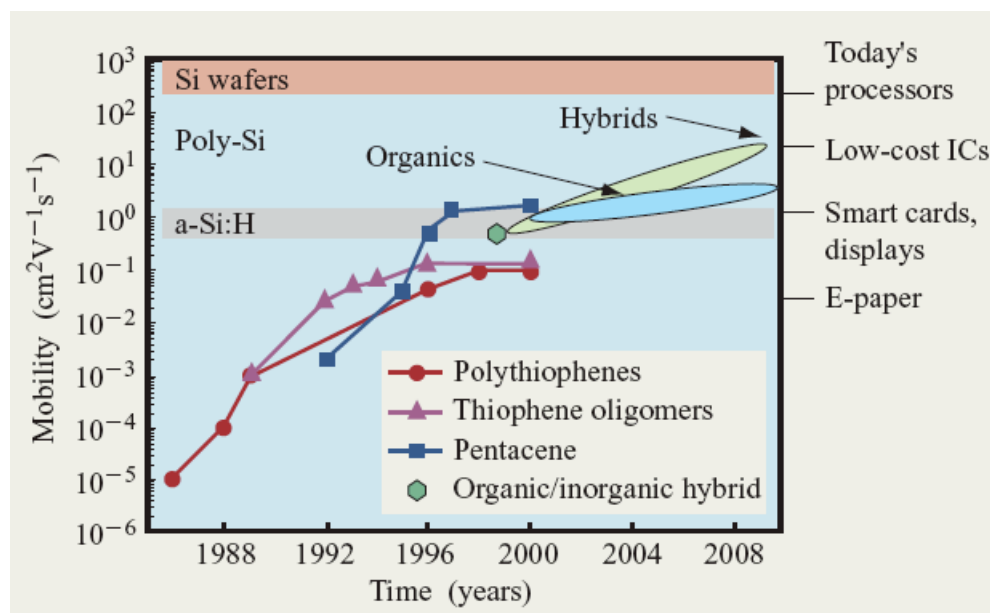


Figure 1. Organic and inorganic semiconductor mobility improvement over time [2].

## Organic Semiconducting Materials

Two organic material categories exhibiting semiconducting properties are polymers (e.g. regioregular poly(3-hexylthiophene) (P3HT)) and small molecules (e.g. pentacene), both of which are included with their chemical structure in Fig. 2. Charge transport (i.e. conductance) in these materials is due to the  $\pi$ -orbital overlap of neighboring molecules. This overlap is enhanced—and mobility is improved—through self-assembly and ordering. Additionally, these materials exhibit great mechanical properties such as flexibility, toughness, and the ability to be processed in solution at low temperatures, resulting in new manufacturing processes such as roll-to-roll and ink jet printing. Recently, On/Off current ratios of P3HT and pentacene have reached as high as  $10^6$  and  $10^7$ , respectively. Additionally, mobilities (see Fig. 2) have been good enough for circuits running at a few MHz and demonstrated with over 1000 transistors.

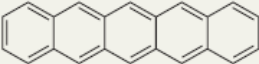
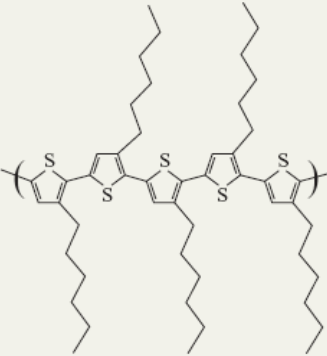
Semiconductor	Representative chemical structure	Mobility ( $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ )
Silicon	Silicon crystal	300–900
	Polysilicon	50–100
	Amorphous silicon	~1
Pentacene		~1
Regioregular poly(3-hexylthiophene)		$10^{-1}$

Figure 2. Common semiconductor materials, their chemical structure and mobility data [2].

As it will be employed and applied in our lab, P3HT is miscible in certain solvents and exhibits moderate but repeatable charge carrier mobility when layers are spin-cast. The polymer chains align themselves as shown in Fig. 3 where **a** and **b** represent the spacing among neighboring chains. The quality of the P3HT layer is dependent upon the materials at its interface(s) and the method with which it is applied.

Aside from the semiconductor itself, the gate insulator material and electrode architectures are of great importance in OTFTs. A common device layout employs a bottom-gate architecture as depicted in Fig. 4(a). In short, the application of the insulator and the interface between it and the semiconductor greatly affects the overall device performance. An additional

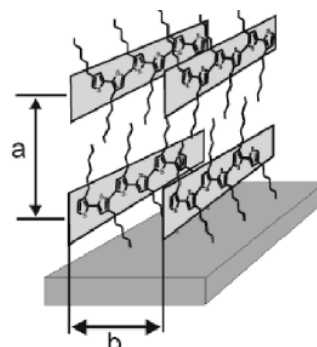
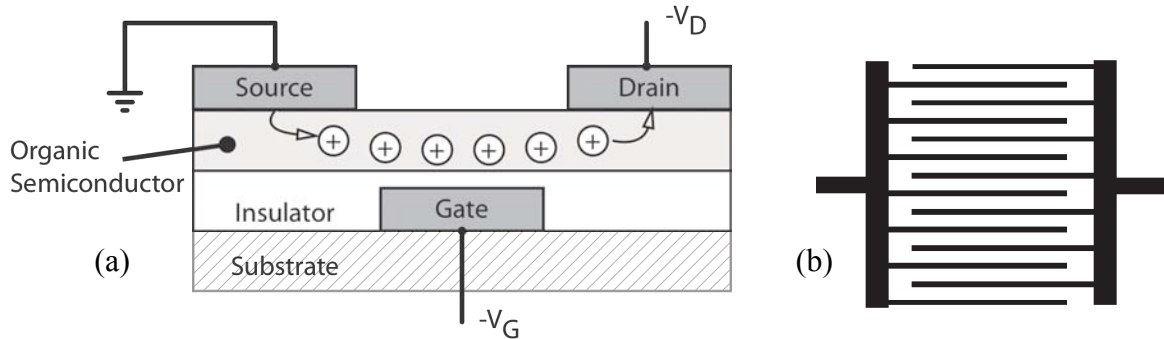


Figure 3. Structure of P3HT following spin-casting.

hurdle introduced with the bottom-gate architecture is the application of the source and drain electrodes on *top* of the semiconductor layer. This makes patterning difficult but keeps contact resistance lower. In this lab (see Fig. 6), we will attempt to bypass these issues in the following two ways: by using spin-castable P3HT as our semiconductor, allowing for simpler application of a polymer gate insulator (polyvinyl propylene (PVP)) also by spin-casting; and by using a top gate architecture, allowing us to pattern the source and drain electrodes in an interdigitated form as shown in Fig. 4(b). This pattern effectively increases the channel width, thus leading to higher currents. In addition, by applying the insulator as the top layer, we can use a liquid metal (gallium-indium (GaIn) eutectic) as the gate electrode in an unpatterned, single contact point.



**Figure 4. (a) Diagram of a bottom-gate OTFT device showing the path of charge carriers from source to drain; (b) Interdigitated pattern for source and drain electrodes.**

## OTFT Operation and Characterization

An inorganic metal-insulator-semiconductor field-effect transistor (MISFET) is a three-terminal device in which the source and drain contact the bulk semiconductor solid with the gate separated by an insulator. Proper doping creates p-n junctions in the bulk and an applied voltage on the gate can create an inversion region beneath the gate insulator within which charge carriers move between source and drain, providing a current modulated by the magnitude of the gate voltage. OTFTs are similar in that current between the source and drain electrodes can be modulated by the gate voltage. However, the semiconductor in an OTFT is just as the name implies, a thin film, not a bulk solid. Additionally, there are no p-n junctions. Instead, the metal electrodes easily inject charge into the semiconductor meaning the operation of the device, i.e. the regime in which current enhancement is appreciable, occurs in accumulation, not in inversion.

Current in an OTFT, as shown in Fig. 4(a), arises from two processes: a bulk current that is present even without an applied gate voltage and a field-effect current that increases as a potential appears on the gate electrode, causing accumulation of carriers in the semiconductor. Because of this, an *n*-channel OTFT contains an *n*-type semiconductor and a *p*-channel OTFT contains a *p*-type semiconductor.

Characterization of an OTFT and its operating regimes is similar to that of a MISFET in that the important measurements concern the drain current. Figure 5(a) presents drain current vs. drain-source voltage for a P3HT OTFT with a grounded source electrode. A transition in the current as it approaches the saturation regime is especially apparent in the  $V_{GS} = -40$  V curve. Additionally, the application of negative drain and gate voltages and a resultant negative drain

current reveals this to be a *p*-channel device, i.e. holes are the charge carriers. Figure 5(b) is the drain current vs. gate-source voltage for the same OTFT. A threshold voltage can be extracted from the data (as will be done in this lab) and a current increase of four orders of magnitude is apparent.

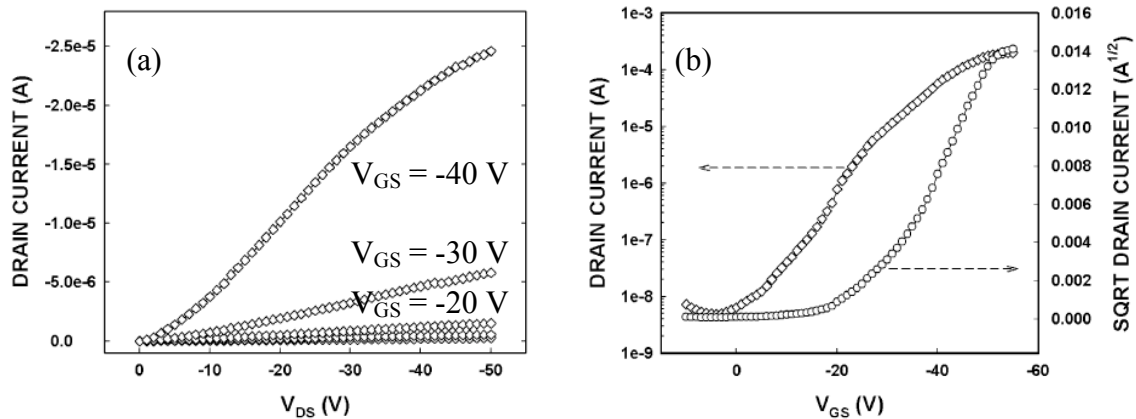


Figure 5. (a) Drain Current vs. Drain-Source voltage and (b) Drain Current vs. Gate-Source Voltage of a P3HT OTFT on a paper substrate (grounded source) [3]

### Construction of an OTFT

In this module, we will fabricate an OTFT, with the construction shown in Fig. 6. We will begin with two glass substrates coated with transparent and conductive indium tin oxide (ITO). One of these substrates will be pre-patterned via photolithography as in Fig. 4(b) and will act as the source and drain electrodes and the other will act as the gate electrode. To the patterned substrate we will first spin-cast the semiconductor layer, P3HT, followed by the insulating layer, PVP. To the second substrate we will apply a small amount of gallium-indium (GaIn) eutectic surrounded by optical adhesive to provide good mechanical contact to the insulating layer.

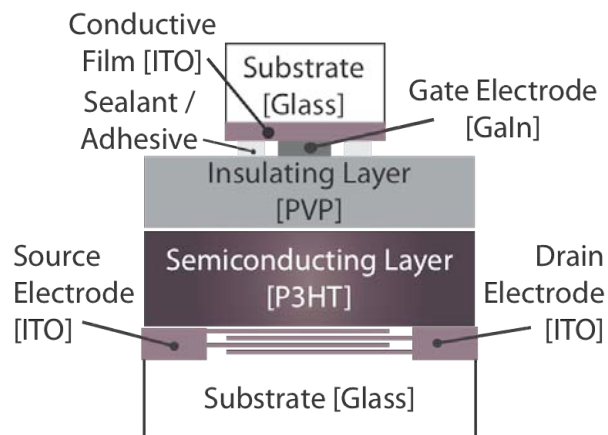


Figure 6. Fabrication Layers of OTFT.

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## Experimental Procedure

### Important Notes:

- The option exists to perform this lab within a Glovebox designed to effectively evacuate harmful vapors, to provide a controlled environment in which to construct devices, and to provide a constant flow of nitrogen when necessary. Such is a good alternative to a fume hood or other controlled environment.*
- Follow all of the instructions and precautions of your lab director(s) as variations from the procedures below may be in place.*
- Always hold your samples along the edges and not by the flat faces.*
- Always keep the ITO side of the substrates facing up.*
- See Appendix for the spin-casting parameters and material recipes.*

### Part 1 – Semiconducting and Insulating Layers

#### EXPERIMENTAL OBJECTIVE:

To apply the semiconducting and insulating layers of the OTFT (P3HT and PVP) onto the patterned substrate.

#### Procedure

1. Prepare your Lab Notebook:
  - a. Fill in your lab notebook headings (Lab #, Station Name, Page #, Name, Date).
  - b. Briefly record the objective of this experiment.
  - c. Sketch the complete cross-section of the OTFT we are creating in this lab.
2. Prepare the Patterned Substrate:
  - a. Use a Multimeter (or similar device) in resistance mode to find the conductive side of the ITO-coated glass. The ITO side should measure a resistance of below 1 k $\Omega$ .
  - b. Clean the substrate using an air gun and **methanol**.
  - c. Transfer the substrate to a hotplate set at 140 °C.
3. Spin-Cast the Layers:
  - a. Secure the substrate in the spin-caster and, using a syringe and 0.45  $\mu\text{m}$  filter, place 8-12 drops of **P3HT solution** onto the substrate.
  - b. Run Program F (see Appendix) unless instructed otherwise.
  - c. When complete, place the substrate on a hotplate (140 °C) to dry for ~10 minutes.
  - d. Return the substrate to the spin-caster and, using a syringe and 5  $\mu\text{m}$  filter, place 5-8 drops of **PVP solution** onto the substrate.
  - e. Run Program G (see Appendix) unless instructed otherwise.
  - f. When complete, place the substrate on a hotplate (140 °C) to dry for ~10 minutes.

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## Part 2 — Create the Gate Electrode and Assemble the OTFT

### EXPERIMENTAL OBJECTIVES:

- (1) To create the gate electrode consisting of Gallium-Indium Eutectic, optical adhesive, and ITO-coated glass.
- (2) To adhere the gate electrode to the P3HT & PVP coated, patterned substrate.

### Procedure

1. Prepare your Lab Notebook as before.
2. Create the Gate Electrode :
  - a. Using a cotton swab applicator, apply a *small* quantity of GaIn Eutectic near the top of a 1/3" X 1" piece of ITO-coated glass. *Be sure to check which side is ITO-coated!*
  - b. Using the syringe filled with optical adhesive, loosely encircle the GaIn spot.
  - c. You should now have a gate electrode as drawn in Fig. 7(a) below.
3. Create the OTFT:
  - a. Hold the patterned substrate at a low angle to overhead light so as to make the electrodes visible. With a permanent marker, place an alignment mark on either side of the interdigitated pattern *on the underside of the substrate* as shown in Fig. 7(b) below. Place this substrate on the worktable.
  - b. Invert the gate electrode from Procedure 2 and gently place it onto the patterned substrate so that the GaIn spot is between the alignment marks.
  - c. Apply gentle pressure with a cotton swab applicator to spread the GaIn.
  - d. Using the UV light, cure the optical adhesive for ~1 minute. *Be sure to have on your safety goggles in order to block the UV light from your eyes!*
  - e. You should now have a completed and cured OTFT as drawn in Fig. 7(c).

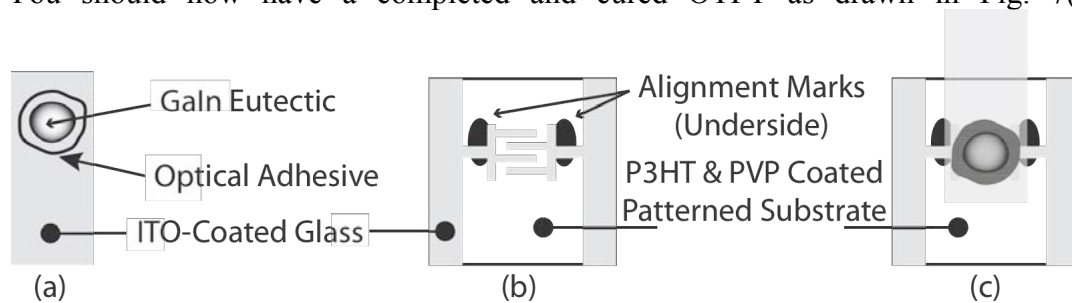


Figure 7. The OTFT Construction Process: (a) The gate electrode; (b) The alignment marks; (c) The completed device.

### Calculations/Questions (Part 2) These are to be written in your Lab Notebook.

1. Estimate the total surface area of your gate electrode (the GaIn spot size).
2. Describe any difficulties you had in constructing your device. Can you discuss any alternatives?

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### Part 3 — Device Characterization

#### EXPERIMENTAL OBJECTIVE:

Characterize the OTFT by obtaining and plotting current-voltage data.

#### Procedure

1. Prepare your Lab Notebook as before, ensuring to sketch the characterization set-up.
2. Prepare the Source-Drain (SD) and Gate (G) Power Supplies and Connect the OTFT to the Characterization Set-Up:
  - a. With power supplies *not* connected, turn them ON and set to 0V. Turn them OFF.
  - b. Attach the RED clip from the SD supply to one side of the patterned substrate and attach the BLACK clip from the SD supply to the other side. Be sure to make good contact with the ITO portions of the pattern.
  - c. Attach the RED clip from the G supply to the gate electrode. Be sure the clip does not make contact with the patterned substrate.
  - d. Turn ON both power supplies and turn ON the picoammeter.
3. Obtain Current-Voltage Data:
  - a. Measure the Drain Current ( $I_d$ ) vs. Source-Drain Voltage ( $V_{sd}$ ) and Gate Voltage ( $V_g$ ) for a wide range of voltages in a table as below. The ranges you choose will depend on the performance of your device. *Suggested* ranges are 0-80 V in steps of 20 V for  $V_{sd}$  and 0-80V in steps of 20V for  $V_g$ . Aim for 25 – 30 data points.
  - b. When finished, return OFF the supplies and meter and remove your OTFT.

SD Voltage (V)	G Voltage (V)	SD Current (nA or $\mu$ A)
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#### Calculations/Questions (Part 3)

These are to be written in your Lab Notebook.

1. Create the following plots, and insert them into your Lab Notebook using tape or glue:
  - a.  $I_d$  (vertical) vs.  $V_{sd}$  (horizontal) for different values of  $V_g$  (on the same plot).
  - b.  $I_d$  (vertical) vs.  $V_g$  (horizontal) for different values of  $V_{sd}$  (on three individual plots).
2. Can you identify a turn-on voltage or a saturation voltage from your data?

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## Appendix A: Lab Notebook Guidelines

1. **Do** record entries *legibly, neatly*, and in *INK*.
2. **Do** sign and date every page.
3. **Do** fill in headings completely (Lab #, Station Name, Page #).
4. **Do** record your experimental objective and describe your experiment.
5. **Do** record your experimental setup, data, and all calculations in such a way that someone else could duplicate/verify your steps.
6. **Do** include extrinsic materials by **tape** or permanent glue (staples are acceptable but not preferred). This includes all raw data from recording instruments (e.g., microscope photos), **computer generated graphs**, drawings, specification sheets, etc.
7. **Do** work in chronological order, i.e., **Do Not** skip parts unless specifically told to do so.
8. **Do Not** erase or remove material. If you mess up, simply cross it out and start again! This is part of the experimental process. We will provide you with as many sheets as you need.

## Appendix B: Spin-Caster Parameters

- The following programs were created on a *Laurell Technologies Model WS-40B-6NPP/LITE* Spin-Caster. Other spin-casters can be used but the lab director should ensure the parameters result in quality films.

### Program F

Single Stage: Speed 3000 rpm  
Acceleration 3570 rpm/second  
Time 30 seconds

### Program G

Single Stage: Speed 4000 rpm  
Acceleration 3570 rpm/second  
Time 30 seconds

## Appendix C: Semiconductor Preparation Instructions

- The following instructions employ the following:

COMING SOON

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## Appendix D: Insulating Polymer Preparation Instructions

- The following instructions employ the following:

COMING SOON

## Appendix E: Adhesive Material Preparation Instructions

- The following instructions employ:
  - 3 mL Syringes with Luer-Lok Tips, *Catalog No. 14-823-41*, distributed by Thermo Fisher Scientific, Inc., Pittsburgh, PA, USA.
  - Precision Dispense Tips, *Part No. 5123-B-45*, distributed by EFD, Inc., East Providence, RI, USA.
  - Ultraviolet-Curable Optical Adhesive, *UVS 91*, distributed by Norland Products, Inc.

A single 1 gram bottle of optical adhesive will be enough for thousands of OTFTS. A syringe of the mixture as described below will be adequate for hundreds.

### Adhesive

1. Insert ~4 mg of the adhesive into a 3 mL syringe and remove most of the air with the plunger.
2. Screw a dispensing tip onto the syringe.
3. Wrap syringe with aluminum foil to prevent penetration by ultraviolet light.
4. Adhesive will expire on date marked on the original optical adhesive bottle.

## Appendix F: Material Recommendations

- **ITO-Coated Glass Substrates:** *Part No. CG – 90IN – 0110*; 25 x 25 x 0.8 mm unpolished float glass, SiO<sub>2</sub> passivated, indium tin oxide coated one surface, R<sub>S</sub> = 70 – 100 ohms; distributed by Delta Technologies, Ltd., Stillwater, MN, USA. Two substrates are needed for each single-pixel LCD.
- **Gallium-Indium, Eutectic:** *Item # 495425, 99.99+ % trace metals basis*, distributed by Sigma-Aldrich, Inc., St. Louis, MO, USA. A single 5 gram bottle of Gallium-Indium is adequate for hundreds of OLEDs when used sparingly as suggested in the procedures.

## Appendix G: Relevant Sources (Books, Links, Papers, etc.)

1. G. Horowitz, "Organic Thin-Film Transistors," in *Semiconducting Polymers: Chemistry, Physics and Engineering*, 2nd edition, ed. by G. Hadziioannou and G.G. Malliaras, (Wiley-VCH, 2007), pp. 531 – 566.

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2. J.M. Shaw, P.F. Seidler, "Organic electronics: introduction," *IBM J. Res. & Dev.*, **vol. 45**, no. 1, 2001.
  3. Y. Kim et al, "A strong regioregularity effect in self-organizing conjugated polymer films and high-efficiency polythiophene:fullerene solar cells," *Nature Materials*, **vol. 5**, pp. 197- 203, 2006.
  4. H.E. Katz, "Recent advances in semiconductor performance and printing processes for organic transistor-based electronics," *Chem. Mater.*, **vol. 16**, pp. 4748 – 4756, 2004.
  5. C.R. Newman, C.D. Frisbie, D.A. da Silva Filho, J.-L. Bredas, P.C. Ewbank, K.R. Mann, "Introduction to organic thin film transistors and design of n-channel organic semiconductors," *Chem. Mater.*, **vol. 16**, pp. 4436 – 4451, 2004.