

Printed Circuit Boards

Bypassing, Decoupling, Power, Grounding

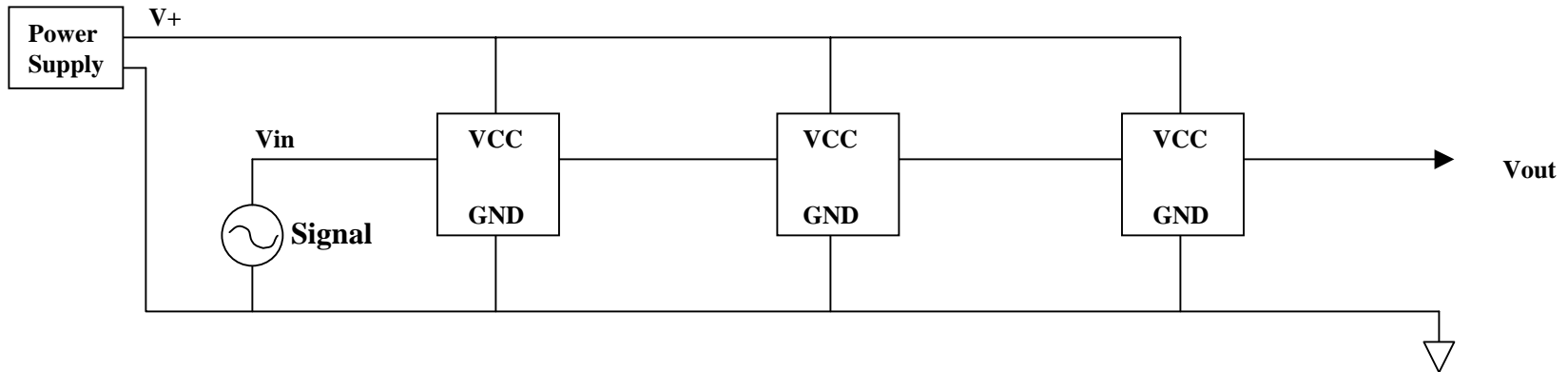
Building Printed Circuit Boards

CAD Tools

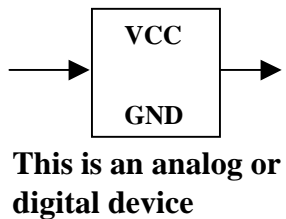
ECE 480/481
Senior Design Project

Bypassing, Decoupling, Power, Grounding

Here is the circuit we want

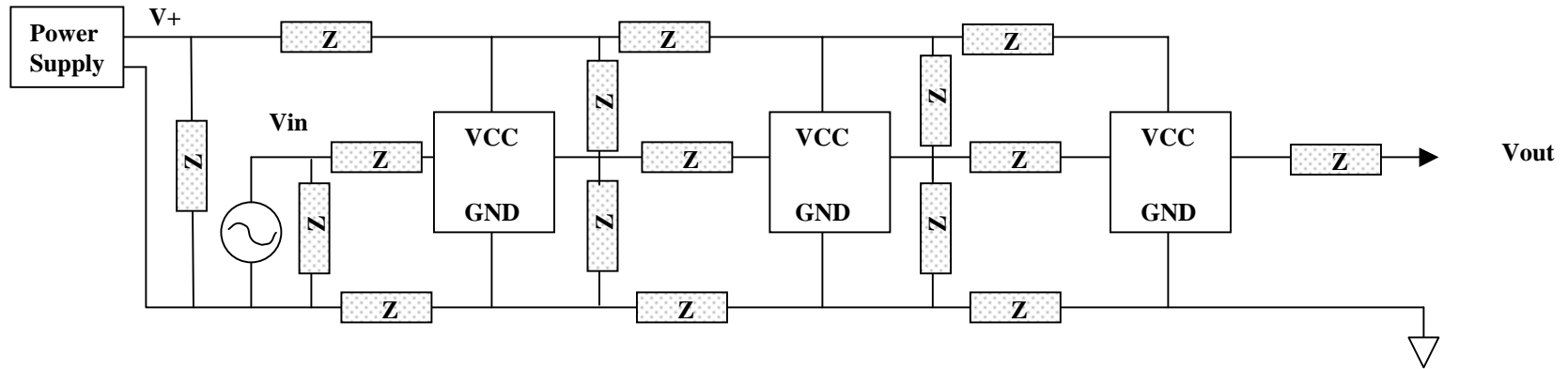


Problems:



- **Devices are not ideal**
 - There is coupling between signals and VCC/GND
- **Connections have finite dimensions**
 - resistance, capacitance, inductance
- **Power and Signal sources have non-zero source impedance**

Here is the circuit we get

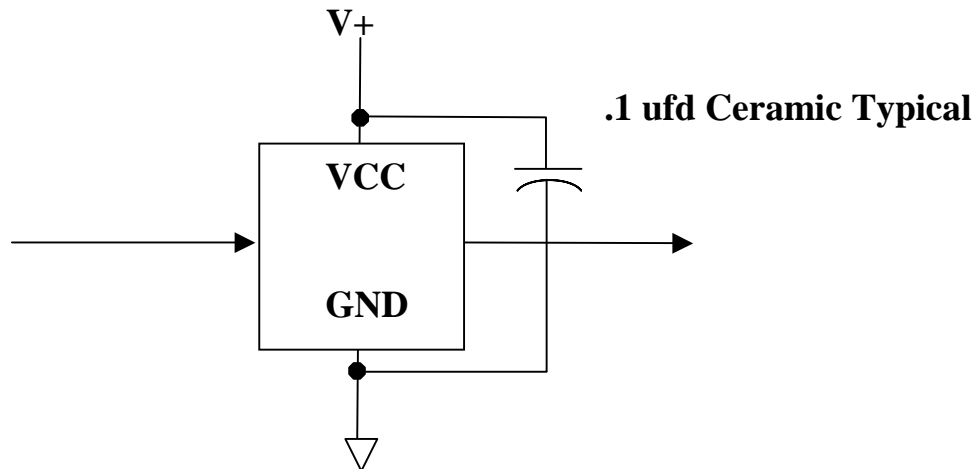


- **Z's have unknown impedance (or hard to determine) values**
- **Z's are complex (frequency sensitive)**
- **Z's are dependent on signal levels, power, dimensions of PCB traces and other factors**

Here's what we do

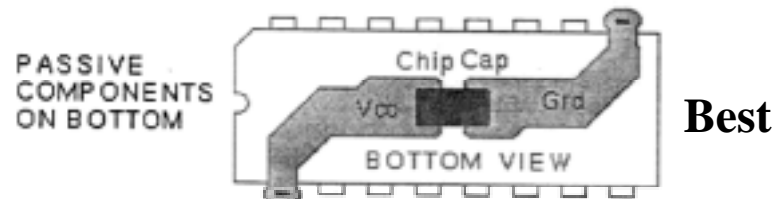
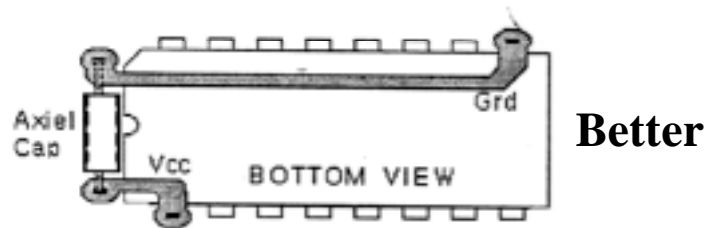
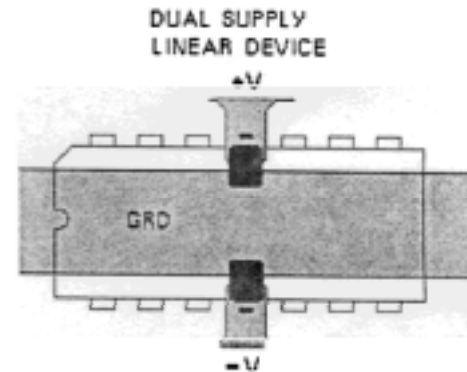
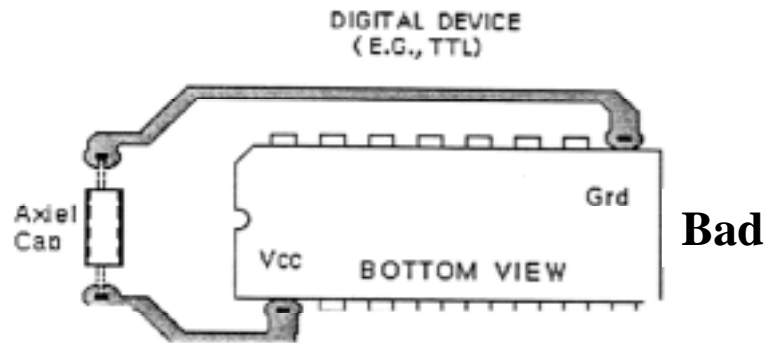
- **Try to make the DC power source to each active device as “clean” as possible**
 - **Bypassing, “short” non-DC components to ground**
 - **Decoupling, “filter” non-DC components from devices**
- **Provide separate grounds between analog and digital circuits**
- **Isolate analog and digital circuits**
- **For noise sensitive signals use differential signaling to cancel common mode noise**

- **Bypass Capacitors**
 - Very high impedance at DC
 - Low impedance to high frequency noise



- Works well for digital and “low noise” analog
- See recommendations in manufacturers data sheets

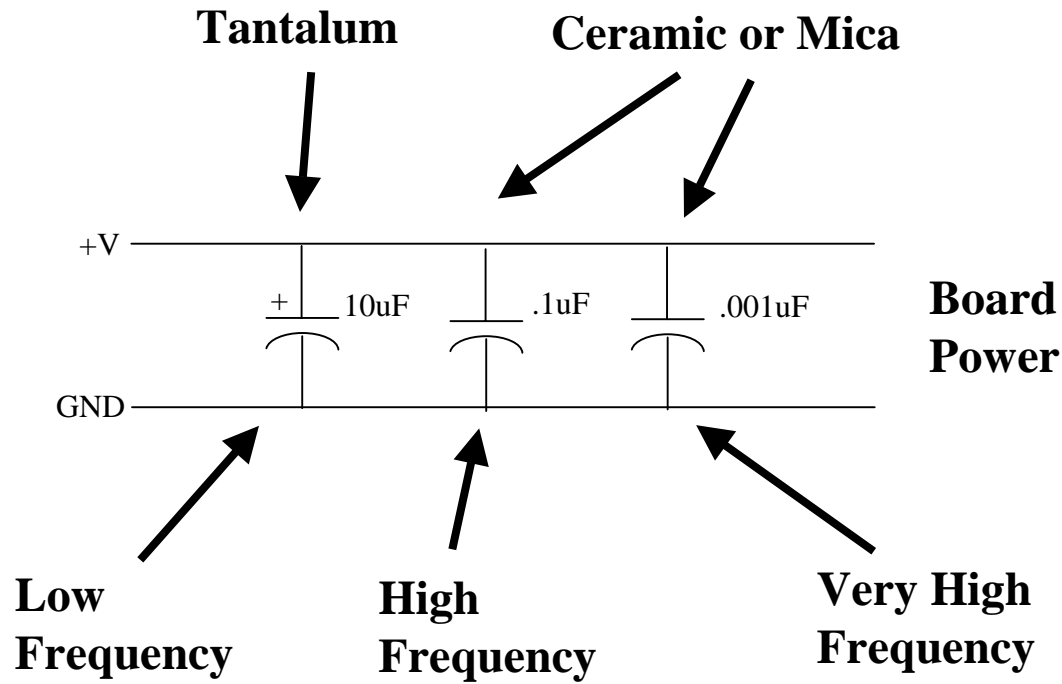
Bypassing - Physical Layout



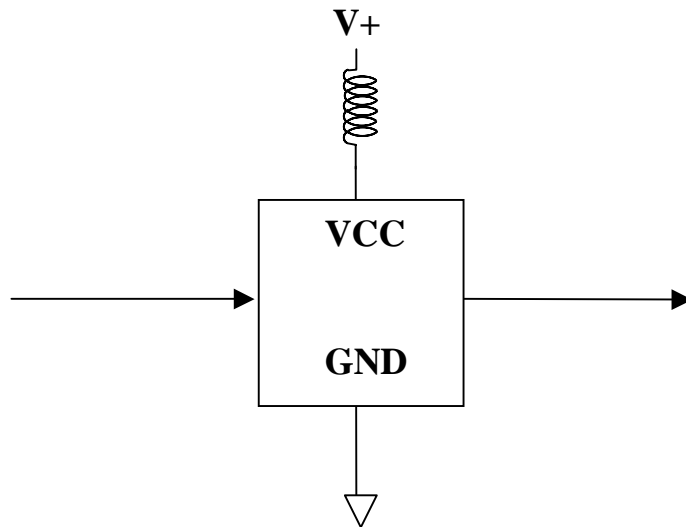
Bypassing Tips

- **.1 ufd or greater, ceramic or mica capacitors (SMT preferably)**
- **One capacitor per SSI, MSI TTL device**
- **Capacitors should connect Vcc and Gnd of the device (shortest path)**
- **Ceramic chip capacitors have good high frequency characteristics, i.e., have small inductance and stray capacitance over a wide frequency range**
- **Tantalum capacitors are a good adjunct to the ceramic. They offer low impedance to the lower frequencies**
- **In some high frequency analog (RF) or high speed digital circuits, it is appropriate to use several different types of capacitors. Tantalum for low frequencies; large ceramic (e.g., 0.1 ufd) for the higher frequencies, and small ceramic, RF capacitors (~1nfd) for the much higher frequencies.**

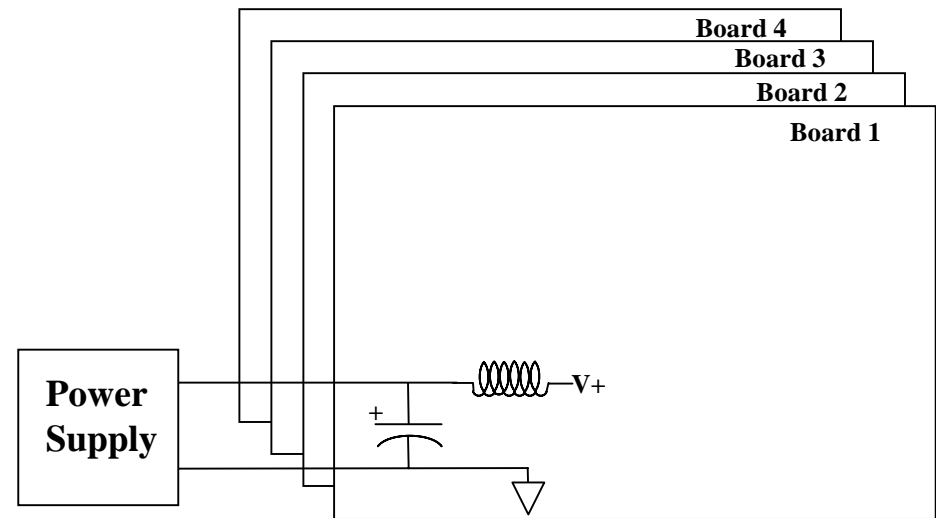
Bypassing Tips



- **Active decoupling**
 - Place voltage regulators on each board, voltage or sub-circuit
 - Expensive and only required in very critical applications
- **Passive decoupling**

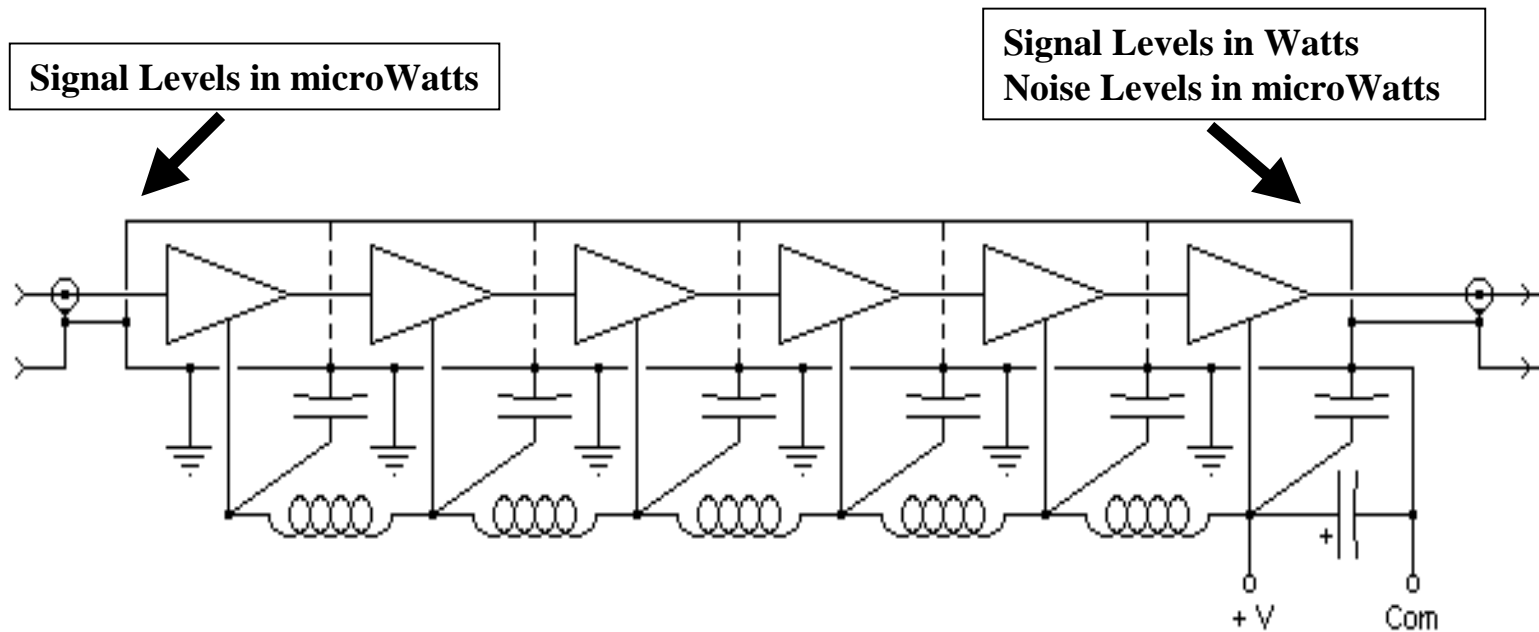


Decoupling on each active device
in high gain environments



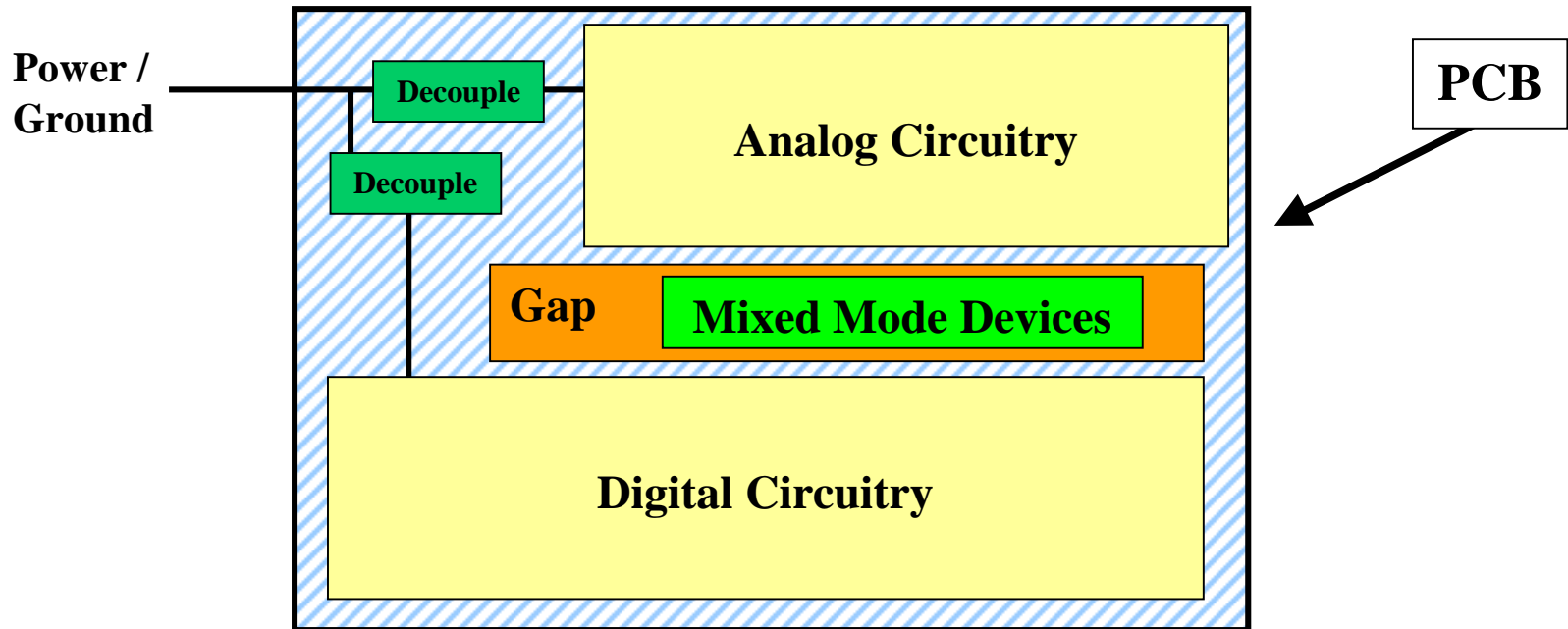
Multiple Board / System Environment

Decoupling -Example



- **Typical IF Amplifier Stages in a Receiver**
 - Very high gain from input to output
- **Decoupled Power Supply at each stage**

- **Passive decoupling is used when voltage regulation is impractical (cannot live with voltage drop) or too expensive**
- **Requires high “Q” components**
 - **Capacitors with low inductance**
 - **Inductors with little distributed capacitance**
- **Values are highly circuit dependent on circuit**



- **Layout Analog and Digital circuits in separate sections of the board**
- **Make separation between sections**
- **Mixed Mode Devices (A/D, D/A) on edge of each section**
- **Decouple Analog / Digital Power to each section**

- **Pay attention to Power and Grounding in your design**
- **“Design-in” bypassing and decoupling from the beginning**
- **More tips on bypassing, decoupling, shielding, grounding, layout and other similar issues on the ECE480 Web page under “Design Reference Homepage”**

ECE 480/481
Senior Design Project

Building Circuit Boards

Making Blank PCB Boards

- **Breadboards, Digital Logic Board and Wire Wrap Boards**
 - Usually used to verify designs and check ideas
 - Not appropriate for final product with most projects
- **Blank PCB Boards - Some options**
 - Etch boards yourself
 - Quick Circuits Milling machine in BioMedical Lab
 - Send out to AP Circuits

- **Etch boards yourself**
 - **Apply “resist” material to copper-clad board and soak in acid**
 - **Hand Layout**
 - **Use resist pen or resist tape to mark layout on copper-clad board**
 - **Use with extremely simple circuits only**
 - **Kits from standard places (Radio Shack, Newark, etc.)**
 - **Transfer film resist**
 - **Copy layout image onto transfer film using Photocopy or Laser Printer**
 - **Heat transfer to copper-clad board with iron**
 - **www.techniks.com/press-n-peel.html**

Making Blank PCB Boards

- **Milling Machine - Quick Circuits**
 - Use with simple to complex circuits
 - 2 sided, unplated-through-hole
 - Accepts Gerber files from CIRCAD, ORCAD or other package
 - Machine in Biomedical Engineering Lab (4th floor, Daniels)
 - Need to provide your own milling bit

- **AP Circuits in Calgary, Alberta, Canada**
 - **Complex circuits**
 - **2 sided, plated-through-hole**
 - **See www.apcircuits.com**
 - **Use “Prototype Service 1”**
 - **2 day turnaround**
 - **Send 5 design files plus order form electronically (Zipped)**
 - **2 board minimum order**
 - **Set-up fee, per sq in charge, drilling charge, shipping charge**
 - **Use ORCAD for design capture and layout**

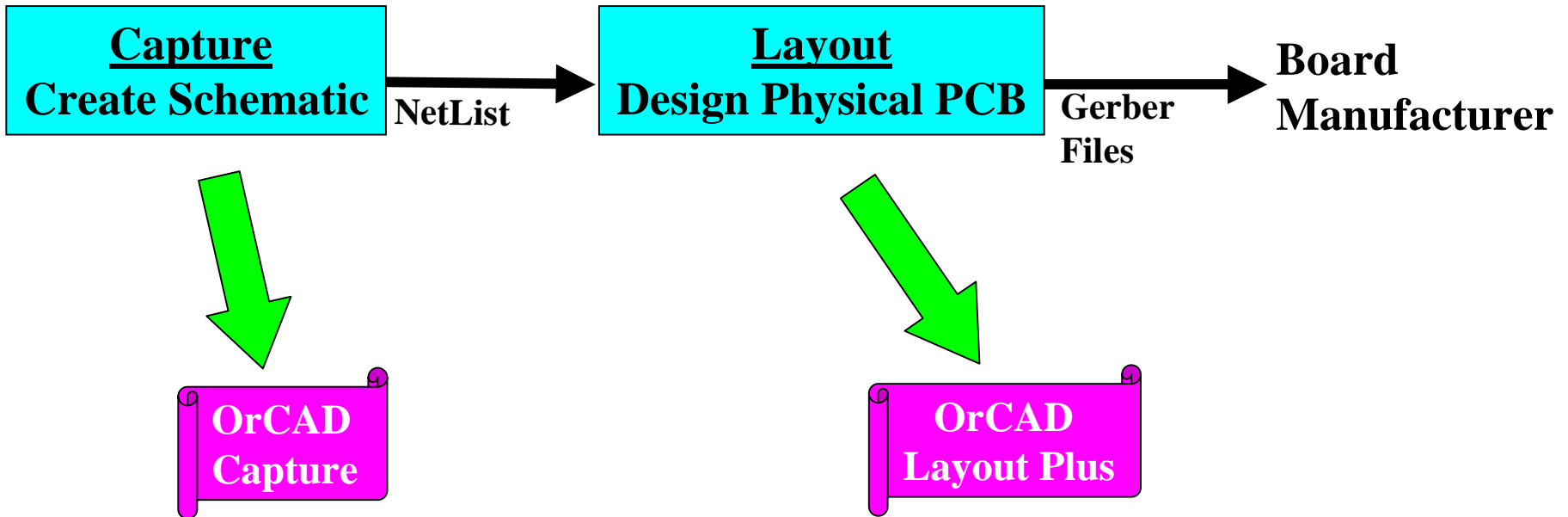
- **Most students hand solder components themselves**
 - Solder tools in Troxler
- **For “difficult” jobs (fine pitch, surface mount, etc.)**
 - **Protronics**
 - <http://www.prototronics-inc.com>
 - **861 Old Knight Road**
Knightdale, NC 27545
Phone: (919) 217-0007
Fax: (919) 217-0050

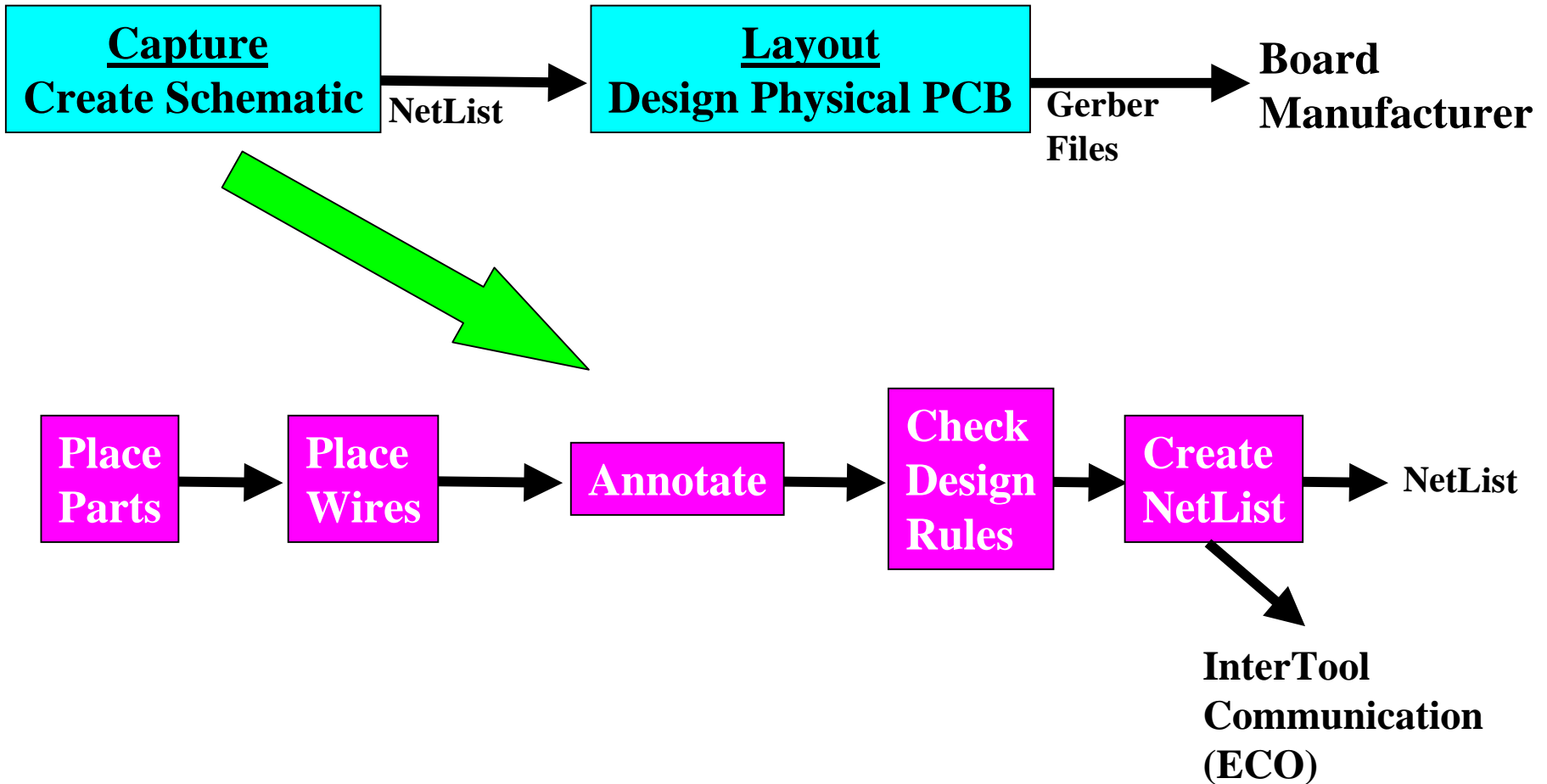
- **CIRCAD (on Quick Circuits machine)**
 - Captures schematic and layouts
 - Library of components
- **ORCAD**
 - Captures schematic and layouts
 - More accepted in industry, bigger library of components
 - Two stations in Troxler design center
 - CAD01 - ORCAD release 9 and older
 - CAD02 - ORCAD release 9
 - Tutorials available on-line

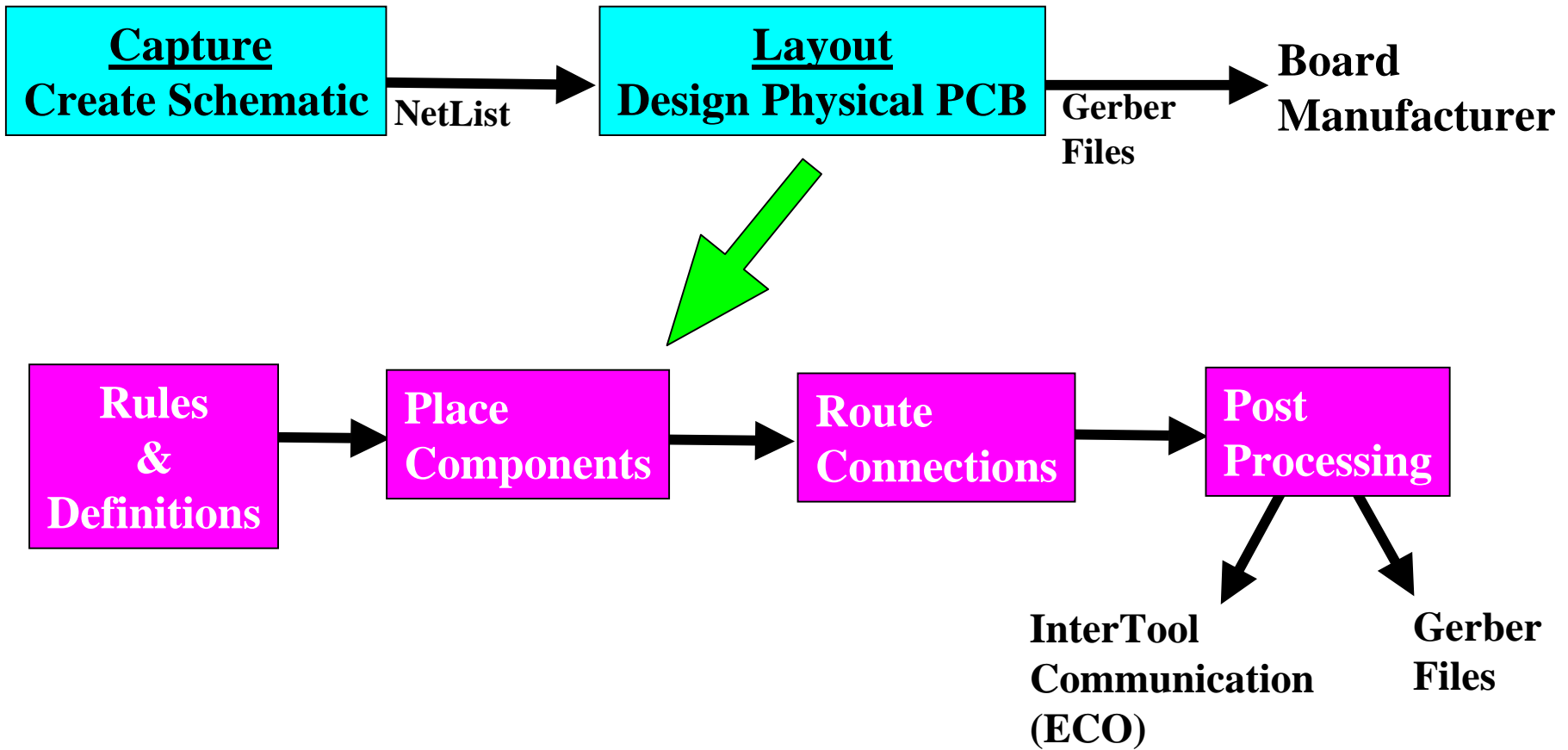
ECE 480/481
Senior Design Project

ORCAD Example

Printed Circuit Board (PCB) Design Process



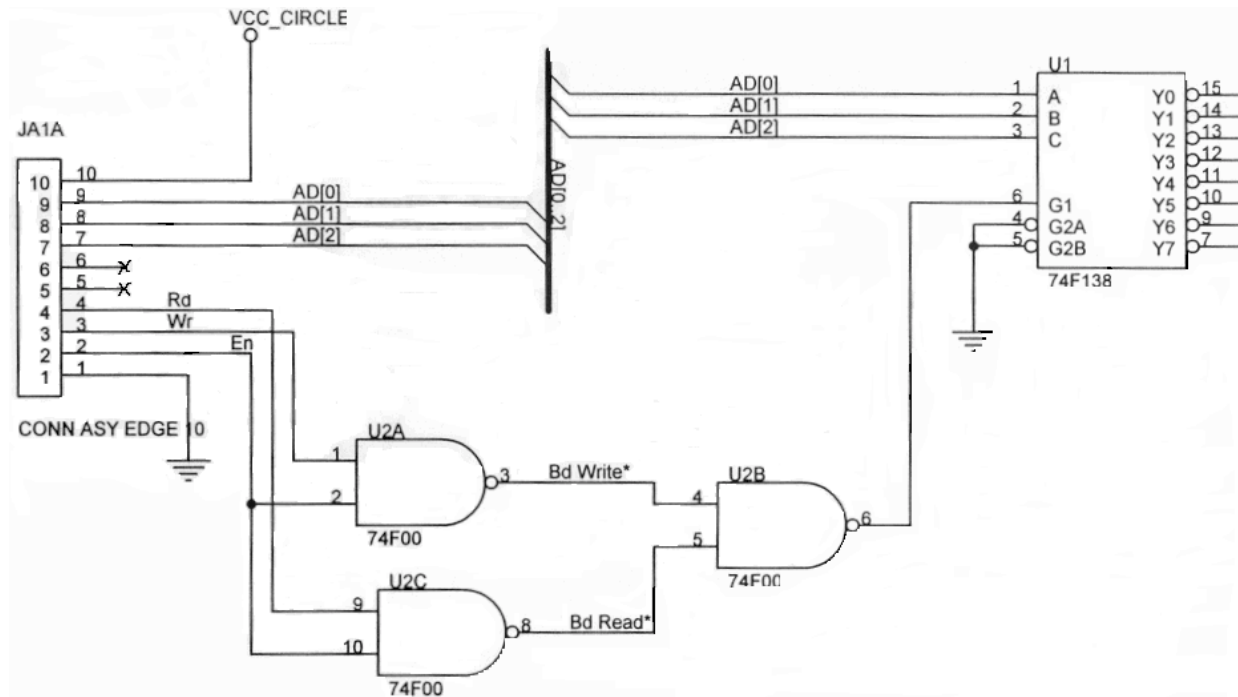




Example for next class

- **Make Schematic and Board Layout for Address Decoder**
- **The following signals are available on a 10-pin edge connector**
 - **Active high read (Rd)**
 - **Active high write (Wr)**
 - **Active high enable (En)**
 - **3 least significant bits of an active high address bus (AD[0..2])**
 - **Power and Ground**

Schematic for Example



A. General layout of screen

1. New > Design

; Project and Schematic Entry windows
; General, Project and Schematic Toolbars
; Net and Net Alias terminology

2. Save As > Users/Bart/ECE480

B. Drawing Schematic

1. Part Placement

Select Parts

; Note Libraries, Labels, Parts/Pkg,
; General n-pin device

Place three, 74F00

Place ConnAsyEdge10

Place 74F138

2. Connecting Parts

Wire Read & Write

Wire NANDS

Place BUS

;Net Alias

Wire BUS to Con/LS138

Wire PWR & GND

;Point out VCC and GND, Net Alias

3. No-connects

C. Schematic Processing

1. Select Project Window

2. Annotate ; Unconditional Update

Note label changes

3. Design Rules Check

4. Generate NetList

NetList > Layout TAB > Check "RUN ECO to Layout"

5. Generate Documents

Parts List

Cross-Reference

D. Session Log

; Note information

A. General Layout of screen

1. **New > 1BET_ANY.TCH > NetList file** ; Technology/Board Templates, Toolbars
2. **Footprints** ; Footprint Library Guide

B. Layout Board

1. Rules and Definitions

- a. **Layers spreadsheet** ; Various sheets
; Make into two layer board
- b. **Draw Board Edge**
Tool > Obstacle > New > Bd Outline ; Obstacle types
- c. **Resize DRC/Route Box**
View > Zoom DRC/Route Box
- d. **Add Mounting Holes**
Component Tool > Pop-up > New ; Point out can add components
Footprints > Layers > MTHole1

2. Place Components

Move around

Rotate ; Select and hit R

3. Routing

Auto > AutoRoute ; Individual Layers, manual routes

C. Layout Processing

1. Auto > Run Post Processor ; Gerber Files

D. Prepare for Manufacture

1. Look at Gerber Files in Windows Explorer

top	Top (component side) foil layer
.bot	Bottom (solder side) foil layer
.sst	Component Legend
.smt	Solder Mask
.app	Aperture File
.drc	Board Outline
.gtd	Gerber Design File