Submit a summary of your on a single sheet of paper, using the template at the end of this homework. Attach any supporting data that you feel you need.

**Question 1**
The purpose of this question is to give you some practice on timing calculations, as discussed in class. Consider the circuit shown below.

Answer the following questions, using the following data:
- Clock skew = 750 ps
- $T_{\text{clock_Q}} = (300 : 450 : 950) \text{ ps in (min:typ:max)}$
- AND delay = $(70 : 120 : 210) \text{ ps}$
- OR delay = $(50 : 110 : 200) \text{ ps}$
- Mux delay from D0 or D1 = $(40 : 90 : 180) \text{ ps}$
- Mux delay from S = $(30 : 80 : 170) \text{ ps}$
- $T_{\text{setup}} = (100 : 200 : 300) \text{ ps}$
- $T_{\text{hold}} = (200 : 300 : 400) \text{ ps}$

(a) What is the fastest possible clock that allows worst-case circuits to work correctly without setup violations? [5 points]

(b) Is there potential for a hold violation (race-through)? [5 points]

**Question 2**
This is a question giving you a brief introduction to Verilog. It also illustrates a “fail-safe” way to code something. If you can not work out how to capture your logical intent in Verilog, then write a truth table and use a case statement.
Consider the following Truth Table (X = don't care, only true and X conditions are shown, all others are false):

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
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</thead>
<tbody>
<tr>
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</tbody>
</table>

Capture the original truth table as a Verilog Procedural Block, using a casex statement. (We have not covered case statements yet, but if you look at the reference guide, and the book if need be, then you should be able to work this out.) [10 points]

**Question 3**
Name 5 newsgroups, email lists, Web sites, or other publicly available electronic resources that can help you with design problems in ASICs or learn more about Verilog and the ASIC design flows in Synopsys/Cadence. (Marketing web sites don't count.) Choose one web-site that is most relevant to your immediate or anticipated job, and say why it is relevant. [10 points]
Name:       Student ID:

I certify that I did not copy the answers to this homework and did not let anyone copy my answers (sign):

Q1. (a) \( t_{\text{clock}} = \)  

   (b) yes  no

Q2.

Q3.