ECE 464, ECE 520 : Digital ASIC Design
Spring 2013
Course Overview & Policies

Class Schedule: Monday, Wednesday, Friday 2.20 – 3.35; EB 2, 1025, as per the class schedule.

Instructor: Professor Paul D. Franzon, Ph.D.
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E-mail: paulf@ncsu.edu
Home page: www.ece.ncsu.edu/erl/faculty/paulf.html
Office Hours: Mon 5.30 – 6.30 (EB2 2116), Wed, Fri in class (see schedule first – days marked with “OH”).

Class Web Site: I am mixing a Moodle site http://moodle.wolfware.ncsu.edu/course/view.php?id=33910 with a custom site http://www.ece.ncsu.edu/asic/2013/index.htm. The Moodle site is meant to be the class main gateway.

Lab TAs/Graders: To be announced on web site.

Class Format and Schedule: There are three levels of learning – memorizing, understanding and applying. A core goal in this class is to get to the highest level as quickly as possible. Towards that goal, the class has been reformatted this semester into a mixed format including pre-recorded material, classroom sessions focused on the application level, peer-learning, on-line experiences, etc. The intent is to use a mixed format to efficiently get you to the highest level as quickly as possible and to leave as much time for the project as possible. Feedback on these practices will be sought during the semester.

Thus we will not be meeting for every scheduled class. Which slots to be used will be announced on the class website. In general we will meet once a week, in order to answer any questions and to conduct in-class exercises, the results of which are discussed in class and turned in formally a couple of days later.

Communications: Students are strongly encouraged to use the Bulletin Board Forums for questions that are not considered “private”. If the question is a good discussion topic, or one that a peer can answer, myself and the TAs might not specifically respond unless it is clear the discussion is not solving it. However, if it is clear that the questions can only be answered by one of us, we will do so as soon as practical. TA-manned Labs should be used for problems related to CAD tool and code debug issues. For addressing issues that the above methods are not suited for, email is preferred over the telephone.

Labs. Regular TA-manned labs will be established. You will find these very useful for resolving design and tool questions and should be your primary method to do so.

Class Attendance. On campus students are expected to come to attend the “live” classes. Students will be called by name to present solutions to problems being discussed. In addition, material covered in these classes is considered examinable, even if there are no electronic records of that material.

Textbooks & Notes:
Purchase is Optional.

- D.R. Smith and P.D. Franzon, "Verilog Styles for Synthesis," (Pearson Education [Prentice Hall]), 2000. ISBN. 0-201-61860-5. The chapters on design, timing, test benches are lifted straight from this course.
- Course notes, etc. on class web page.
- References:

You will find the course website and bulletin board on wolfware, as linked from the page www.courses.ncsu.edu/ece520. I emailed the class earlier this week. If you did NOT receive these emails, check your “official” email address at www.ncsu.edu under “directories” in the top right corner, and update it if need be.

Prerequisite: Grade of C or better in ECE 212 or equivalent. ECE 406 is useful but not assumed. Functionally, I assume that students are familiar with logic design, including combinational logic gates, sequential logic gates, timing design, Finite State Machines, etc. If you have never designed and verified even a small digital circuit, and remember the principles by which they work, you will be seriously disadvantaged in this class. I do not assume knowledge of Verilog.

Course Objectives
1. To prepare the student to be an entry-level industrial standard cell ASIC or FPGA designer.
2. To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation, including timing, performance and power optimization, verification and manufacturing test.

Course Outcomes
1. Students will be able to design and synthesize a complex digital functional block, containing over 1,000 gates, using Verilog HDL and Synopsys Design Compiler.
2. Students will demonstrate an understanding of how to optimize the performance, area, and power of a complex digital functional block, and the tradeoffs between these.
3. Students will demonstrate an understanding of issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.

ECE 464 or ECE 520? ECE 520 has wide recognition for preparing ASIC designers for industry. ECE 464 does not. If you are interested in gaining a “job qualification”, and found ECE 406 straightforward, I’ll advise you to take ECE 520, rather than 464. However, the ECE 520 project is an order of magnitude more difficult than the 464 project and includes a strong design optimization component. The 464 project does not require much optimization.

Course Approach:
Recorded Lecture Materials: Designed to prepare you for the project and cover issues important to ASIC designers. Classes: Classes include pre-announced activities designed to help you achieve the application level of learning. Attendance and participation are expected. Laboratories: A lab schedule will be established. Though lab attendance is not required, you are strongly encouraged to use the help available in the labs to sort through homework and project issues. In fact, only minimal help will be available outside the laboratory times. Quizzes: There are two levels of quizzes built into the pre-recorded material. Each module is broken into small segments with a quiz at the end of each segment. This quiz is simply to provide you with feedback on the knowledge and understanding you gained in that segment. Though your scores are recorded, they do NOT become part of your grade. There is an additional quiz at the end of each module. This score is also recorded and DOES become part of your grade.
Homeworks: The homeworks are designed to either help you gain the skills required for the project or to help prepare you for the exams. Collaboration is encouraged though each student is expected to turn in individual solutions.
Written Exams: There will be two written exams, a one hour midterm and a three hour final. Both are comprehensive, open-book, open-notes exams.

Course Syllabus
0. Revision of Digital Design
1. Introduction to ASIC design
2. Timing design
3. Design of digital hardware using Verilog HDL I
4. Design of digital hardware using Verilog HDL II
5. Design of Finite State Machines
6. Design of complex systems.
7. Managing hierarchy.
8. Verification.
10. Low Power Design.
11. Introduction to FPGAs
12. Future issues

Homework TurnIn
  o On-campus students. The quizzes are conducted and evaluated on-line. The homeworks can be turned in
  on-line or brought as paper to class.

Student Evaluation

<table>
<thead>
<tr>
<th>Item</th>
<th>Date</th>
<th>ECE 520</th>
<th>ECE 464</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homeworks &amp; End of Module quizzes</td>
<td>February, 20</td>
<td>25%</td>
<td>25%</td>
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<tr>
<td>Midterm Exam</td>
<td>February, 20</td>
<td>10%</td>
<td>10%</td>
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<tr>
<td>Project Plan – Prelim Report</td>
<td>March 13</td>
<td>5%</td>
<td>5%</td>
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<tr>
<td>Project – Final Report</td>
<td>April 17</td>
<td>40%</td>
<td>40%</td>
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<tr>
<td>Final Exam</td>
<td>Wednesday, May 8, 1-4 pm</td>
<td>20%</td>
<td>20%</td>
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Each homework and project item can be submitted up to one week late with a 10% penalty. After more than a
week, the item can’t be accepted. Exams are open book, open notes. You may NOT use computers, mobile phones
and PDAs during exams. Though you can collaborate during homeworks, direct copying of solutions, in part or
in whole, is not permitted. All code required for the homeworks should be individually designed and
developed. We will be running code comparison tools on homework solutions, and projects. An Audit requires
completing all the end of module quizzes and homeworks with a grade of at least 80%.

Important Dates
  See Class Schedule

Instructor Research Interests
  o Application specific processors and sensor systems. Current projects are in applications of 3DICs, sensor
  system design, and secure IP design.
  o Interconnect, including transceivers, electronic packaging, on-chip interconnect, and between-chip
  interconnect.
  o Nanocomputing – how to build the computers that will eventually displace or complement CMOS.

Students with disabilities
Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of
available accommodations, students must register with Disability Services for Students at 1900 Student Health
Center, Campus Box 7509, 515-7653. [http://www.ncsu.edu/provost/offices/affirm_action/dss/](http://www.ncsu.edu/provost/offices/affirm_action/dss/) For more information
on NC State's policy on working with students with disabilities, please see
[http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html](http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html)

Academic integrity
All the provisions of the code of academic integrity apply to this course. In addition, it is my understanding and
expectation that your submission of any test or assignment means that you neither gave nor received unauthorized
aid. My policy for homeworks and projects is that while you are free to collaborate, sharing of design data,
specifically Verilog code, is expressly forbidden. If you collaborate on a design problem, I still expect you to
turn in individually developed code.