I/O Circuits

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Global Outline
• Interconnect Structures and Models
• Signaling
• Driver & Receiver circuits

References
• Dally & Poulton, Chapters 3, 5, 6, 7, 8
• With acknowledgements to Lei Luo, Leon Leong, Rizwan Bashirullah
Outline

Driver Circuits
Receiver Circuits
On-chip termination
Equalization DSP alternatives
Drivers

Outline:

- Voltage mode drivers
  - Drive and pre-drive
  - Tri-state
  - Rise time control
  - Self-termination
  - Differential
- Current mode drivers
- Transmitter pre-emphasis
Voltage Mode Drivers

Basic Objectives:

- For $V_{swing} > 0.9 \ V_{dd}$, $R_{out} < 0.1 \ Z_0$
  - $\Rightarrow$ Large drive transistors
  - $\Rightarrow$ Pre-drive circuit needed
    - $\Rightarrow$ Remember ratio’d driver (see CMOS notes)
- Must avoid nFET and pFET being on at same time
  - Otherwise large short circuit current during transition
    - $\Rightarrow$ Break before Make circuit
- Reasonable area
- Small $\frac{di}{dt}$
  - $\Rightarrow$ Rise time control
Basic Voltage Drivers

Techniques to prevent short-circuit current:

<table>
<thead>
<tr>
<th>En</th>
<th>Data</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>:</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>:</td>
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<tr>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
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</tr>
</tbody>
</table>

NAND: \( t_r > t_f \)
NOR: \( t_f > t_r \)
Use rise, fall times to prevent \( I_{sc} \) (beware of process spread)
Reduced tri-state driver:

Same functionality as previous page, with fewer transistors and break-before-make
**Rise Time Control**

**Goal**: Reduce $\frac{di}{dt}$ without significant reduction in delay

- Typically $tr < 0.3 - 0.5 \ t_{\text{bit}}$
- Process, temperature variations ➔ Active control might be desirable (e.g. Use nMOS as pFET and control “resistance”)
- First stage to switch usually the largest

![Circuit Diagram](image-url)
Output Impedance Control

e.g. To precisely match line in series termination

- Digitally trimmed circuit
- NC1, NC2, PC1, PC2 produced by comparing copies of the drive FETs with an off-chip resistor (e.g. voltage division or a bridge)
Current Mode Drivers

Single sided:
- Relies on saturated FET

Requires:
- $V_{out} > V_{DD} - V_t$
- Digital trimming to provide $I_{out}$ across process and temp spreads

Switched Current Mirror
- Series devices must be large
- Small $V_G$ on mirror to max $V_{sw}$

Gated Current Mirror
- Smaller devices
- Slower transient response
Bipolar Current Mode TX

Above Unipolar

- Levels: 0 and x mA

Create bipolar with complementary pull-up of above

- Logic levels = +/- x mA

Example:

![Circuit Diagram](https://example.com/circuitDiagram.png)
**Differential Current Mode TX**

**Current Steering Circuits:**
- Stage 1: Converts large swing to small swing
  - Eliminates dead band at ends of swing in stage 2
    - Output starts to swing as soon as g and g' change
- Second stage loaded with line impedance
  - Often Rload put in parallel to provide source termination
Large Swing Differential Ckts

Design Issues:
- Output Swing
- Input Swing
- Bandwidth
- Source Matching
- Design of constant current sources
- Resistor Design

Can also be used for high speed differential logic (AND, OR, XOR):
Current Mirror

First order treatment

- **M1:**
  - $V_{DS} = V_{GS} \rightarrow \text{Satn}$
  - $I_{ref} = I_{DS} = k/2 \ W/\ L \ (V_{GS} - V_T)^2$

- **M2, M3:**
  - As long as $V_{DS}$ large enough to put into saturation
  - $V_{GS2} = V_{GS3} = V_{GS1}$
  - If $L_1 = L_2 = L_3$, then
    \[
    \frac{I_2}{I_{ref}} = \frac{W_2}{W_1} \quad \frac{I_3}{I_{ref}} = \frac{W_3}{W_1}
    \]

- With Channel length modulation taken into account,
  \[
  \frac{I_2}{I_{ref}} = \frac{W_2/L_2}{W_1/L_1} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} \quad \text{Long L1, L2 improves matching}
  \]
Current Mirrors

(a) \( m_1 \) diode connected & in saturation. When \( m_2 \) in saturation

\[
I_2 = \beta (V_{GG} - V_{tn})^2 (1 + \lambda V_o) = I_1 (1 + \lambda V_o) \quad \text{ro} = \frac{\partial V_o}{\partial I_2} = \frac{1}{\lambda I_1}
\]

- Make transistors long to reduce \( \lambda \)
- Add low pass filter to reduce CM noise from power/ground
- Note: Min voltage drop required over \( V_o \) to keep \( m_2 \) in saturation
**Large Swing Differential Drivers**

**Driver:** Design for Large Swing at output

**DC (Swing) Analysis:**
- M0 must remain in Saturation
  - \( V_p > V_{tn} \) (in 0.18 um, a 0.25 V margin is typical)
- \( ID_1 + ID_2 = I_{tail} \)

Swing limits at output:
- Determine by when M1 or M2 are off
  - \( V_{high} = V_{DD} \)
  - \( V_{low} = V_{DD} - I_{tail} R \)

- Note: M1, M2 must be large enough to support \( I_{tail} \)
- Tradeoffs:
  - Increased swing requires high \( I_{tail} \) ➔ Increased power consumption
  - \( I_{tail} \) limited by requirement: \( V_{low} > V_p \) (see above)
Swing, Bandwidth and Power trade-off

OUTPUT impedance

- \( z = R \) at output High
- \( z = R \parallel |R_{M1} \) at output Low
- Requires High \( R_{M1} \) to balance output impedance, put M1 and M2 into saturation will be best

Lumped model \( \tau = R \times C \) at output, C is the load

- High bandwidth means smaller R
  - That’s smaller output swing
  - Max swing is \( V_x = V_{dd} - I_{tail} \times R \)
- Increase \( I_{tail} \) can improve both bandwidth and Swing
  - But burns more power

Suppose output swing from \( V_x \) to \( V_{dd} \)
**Design Example:**

**Design specs:**
- Input swing range: 1.16 to 1.8V
- Output swing range: same as above
- One transistor goes off at max swing
- Data rate $S=5G$ and Load $C_L=100fF$
- $V_{thn}=0.45V \sim 0.52V$, use 0.5V here
- Overdrive voltage margin=0.25V
- Length (L) of M0, 2 to 3 times of $L_{\min}$ to reduce short channel effect
Design Procedure

Edge Rate

- tR \approx 2.2 \text{ RC}
- Want tR < t_{bit}

\Rightarrow R < \frac{1}{(2.2 \times SC)} = 900 \text{ Ohm}

e.g. Chose R = 800 Ohm

Tail current: Itail = \frac{(1.8-1.16)}{R} = 0.8 mA

Vp:

- Keep M0 in saturation and make sure M1 and M2 can turn off
- To keep M0 in saturation implies V_p > V_t. E.g. V_p = 0.75 V gives 0.25 V of margin
- To turn M1 off, requires V_p > V_{in-low} - V_t = 1.16 - 0.5 = 0.66 V
- V_p \geq 0.75 V
… Design Procedure

M0 Sizing

- W/L to give $I_{\text{tail}}$ at $V_{\text{bias}}$
- Make long to reduce impact of short channel effects

M1, M2:

- To give $V_{\text{out-low}}$ while maintaining $V_p$ and keeping it and M0 in saturation
Design for larger swing

You may want large swing for good SNR

But there are two constraints for large swing:

1. At least:
   - $V_X > V_p$ (swing limit on $V_x$)
   - But $V_p$ has to keep $M_0$ in saturation

2. Better if: $V_X > (V_{DD} - V_{th})$
   - to make $M_1$ in saturation
     - To minimize $C_{gd}$ (Miller effect) and maximize $R_D$ of $M_1$

So, Max swing is

- $V_{DD} - V_p - \text{min} = 1.55 \text{ V}$
- Reaching the limit, usually can’t meet

- $V_{dd} to (V_{dd} - V_{th}) = 0.5 \text{ V}$
- For good performance

- $(V_{DD} - \text{Overdrive})/2 = 0.77 \text{ V}$
  - Suggested typical

Also applies to the other direction of input
Design for smaller swing:

You want small swing for higher bandwidth

- Or less $I_{\text{tail}}$ for low power, smaller $M_0$ size

Constraints:

1. Noise margin, SNR

2. Large $M_1$ and $M_2$ to get a high $V_P$

- To turn $M_2$ off
- For example: $V_p > V_x - V_{th}$, if $V_x = 1.4V$, then $V_p > 0.9V$
- Large $M_1$ and $M_2$ is needed to get a $V_p = 0.9V$, this brings more load to previous stage

Suppose output swing from $V_x$ to $V_{DD}$
Another design example: EX2

- S and C \( \Rightarrow R = 1/(2.5*S*C) = 800 \) ohm
- Tail current: \((1.8-1.16)/R = 0.8\)mA
- \(V_p > \text{Max } (0.25, 0.4-0.5)\)
  - Choose \(V_p = 0.25V\)
- \(V_{bias} = V_{th} + 0.25 = 0.75V\)
  - Leave 0.25V as overdrive margin
- \(V_p \text{ and } V_{bias} \Rightarrow W/L \text{ of } M_0 = 48.6u/0.54u\)
  - Design M0 to get such a tail current
- \(I_{N_{\text{high}}} = 1.3V, \text{ get } W/L \text{ of } M_1 \text{ to make sure } V_p \text{ of } 0.25V \Rightarrow W/L = 4.32um/0.18um\)

Design specs example:
- Input swing range: 0.4/0.45 to 1.35/1.3
- Output swing range: 1.8V to 1.16V
- Data rate \(S = 5G\) and Load \(C_L = 100fF\)
- \(V_{th} = 0.5V, V_{ov} = 0.25V, L = 0.54um\) for M0
**Optimization and Verification: EX2**

- If bandwidth allowed, choose higher R
  - Resulting in more swing
  - Or allowing smaller $I_{\text{tail}}$

- If precise $V_{\text{bias}}$ and low gnd noise are available $\Rightarrow$ choose smaller overdrive margin $V_p$, to get more swing

- Check if M1 and M2 at saturation?
  - $V_{\text{IN high}} - V_{\text{th}} = 1.35 - 0.5 = 0.85 < V_{\text{OUT low}}$ Yes, it’s good.

- Check if M1 or M2 is large enough to carry $I_{\text{tail}}$ when Input is high.
  - Requires: $(V_{\text{IN high}} - V_{\text{th}})^2 W_{M1}/L_{M1} > (V_{\text{bias}} - V_{\text{th}})^2 W_{M0}/L_{M0}$
  - Right=$(0.75-0.5)^2*48.6/0.54=5.6$
  - Left=$(1.3-0.25-0.5)^2*4.32/0.18=7.26 > Left!$
  - $\checkmark$ Left > Right, some margin is left for body effect
Easy Scaling

- **Why scaling?**
  - To drive \( N \) times capacitive load or to provide \( N \) times bandwidth

- **How to scale?**
  - \( R/N \)
  - \( M0*N; M1*N; M2*N \)

- **Scaling effect**
  - \( I_{tail} * N \)
  - Bandwidth\( *N \) or equivalent cap load \( *N \)

- **Why the design can be scaled?**
  - Assume IN/OUT swing range the same
  - It’s all about Remaining \( Vp, I_{tail} * N, \) and \( R_{out}/N \)
Resistor variation

- Resistors vary largely across corners than transistors

- When R increase
  - $V_p$ decrease
  - $I_{\text{tail}}$ remains or negligible decrease
  - Output swing increase
  - $I_{\text{tail}}$ need to be calibrated to compensate R variations
Resistor variation – cont.

- Assume $R_S$ and $R_L$ will vary at same direction linearly
- But since $V_{\text{bandgap}}$ remains same, $R_S I_0$ and $R_L I_2$ will remain constant, as well as output swing
Pre-Emphasis

Simple digital z-domain high pass filter
- Must ensure proper voltage swing

E.g. 2-tap FIR

\[ H(z) = a_0 + a_1 z^{-1} \]

\[ r = -\frac{a_1}{a_0} \]

\[ H(z) = a_0(1-rz^{-1}) \]

\[ H(\omega) = a_0(1-re^{j\omega t}) \]

\[ |H(\omega)| = a_0(1+r^2-2r\cos(\omega t))^{0.5} \]

\[ |H(\omega=0)| = a_0(1-r) = a_0 + a_1 \]

\[ |H(\omega t=n\pi)| = a_0(1+r) = a_0 - a_1 \]

Boost = \( \frac{a_0-a_1}{a_0+a_1} = \frac{1+r}{1-r} \)

HPF if \( a_0 > 0 \), and \( a_1 < 0 \)
Current mode signaling in serial link design

Diagram showing the current mode signaling in serial link design with components labeled as follows:
- IN
- INb
- R
- TX CLK
- Equalization Coefficients
- DFF
- DAC Current source
- Sense Amp Latch
- Recovered Clean data
- Recovered CLK
DAC current source

$I_{DAC} = 0 \sim 15 \times I_{bias}$

4-bit Equalization Coefficient
Voltage Mode Pre-emphasis

Tap weights effectively set by transistor sizes:

- \( a_1 \) tap smaller transistors than \( a_0 \) tap
Tap Sizing

First order design procedure:
If response at end of line to a 010 pulse is:

Then size of taps are \(-a_1, -a_2\) and \(-a_3\) as given above
(i.e. Use taps to subtract this amount from previous “1”s if present).
Receivers:

- Basics on detection and sampling
- Inverters
- Differential
- Clocked differential receivers
  - Integrating
  - Matched filter
Detection & Sampling

Eye requirements at input to RX:

- To meet requirements to sample and amplify signal in presence of noise, timing skew and jitter

\[ \text{skew+jitter} \quad \text{aperture time} = t_{\text{setup}} + t_{\text{hold}} - t_r \]

Why? aperture time = \( t_{\text{setup}} + t_{\text{hold}} - t_r \)

As \( t_{\text{setup}}, t_{\text{hold}} \) measured to 50% points, aperture at top & bottom of eye (at 10%, 90% points)
Detection and Sampling

UI = Unit Interval (bit period)

- Horizontal eye opening specified in UI
  - Typical requirement ~ 0.7 – 0.8 UI
- Templates often used in standards against eye diagram
Detection & Sampling

Alternatives

- Separate amplifier + sampler (i.e. Flip-flop)
- Clocked amplifier (integrated)

- Advantages of clocked amplifier
  - Lower power
  - Jitter contribution of amplifier “portion” reduced
  - More sensitivity
  - Sampling rate not constrained by gain-bandwidth product
**Static (separate) Amplifiers**

**Inverters**
- Gain around $V_{inv} \approx 4/((V_{GS}-V_t)(\lambda_p+\lambda_n))$
- Gain $\approx 20$ for “book” 0.35 µm process
- $\Rightarrow$ Sensitivity $\approx (V_{IH}-V_{IL})/\text{Gain} = 2.5/20 = 125$ mV
- Offset determined variation in $V_{inv}$ with process, temp and $V_{dd}$ variations
  - About 300 mV for process variation
  - About 500 mV including temp & $V_{dd}$ variation
- Not best used for initial gain stage in RX
- Useful for final gain stage, however

**Inverter Variation**
- Schmidt Trigger
  - Hysterisis $\Rightarrow$ very wide NM
Static Differential Receivers

Advantages:

- More sensitive
  - Determined by $gm$ of source coupled pair and $R\Delta$ of load
  - 20 – 100 mV

- Less input offset voltage
  - Determined by nFET, pFET mismatch
  - 10 mV
  - Can be compensated by trim transistors

- Rejects common mode noise at input (i.e. can reject part of received SSN and crosstalk)

FIGURE 4-59. DC Transfer Characteristics of a Source-Coupled Pair

100 mV
**Differential Rx**

**Design Issues:**

- **Differential voltage gain**
  \[ A_d = \frac{V_{\text{out}_P} - V_{\text{out}_N}}{V_{\text{in}_P} - V_{\text{in}_N}} \]

- **Output swing**

- **Common Mode Rejection Ratio**
  \[ \text{CMRR} = \frac{A_d}{A_c} \]
  \[ \text{CM gain: } A_c = \frac{V_{\text{out}_P} + V_{\text{out}_N}}{V_{\text{in}_P} + V_{\text{in}_N}} \]

- **Bandwidth**
Max Swing and Differential Gain

Maximum Swing (on one side)

= $I_{bias} R$ (as before)

Differential gain:
Using Small Swing equivalent circuit

$$|A_v| = g_m(R) \left| \frac{1}{g_{ds}} \right|$$

Assuming IV square law relationship (first order equations)

$$\frac{\Delta I_D}{\Delta V_{in}} = A_{I,DM} = \sqrt{\beta I_{SS} R}$$

$$A_v = A_I R$$

Note: Gain/BW tradeoff, Since both increase with $R$
**CMRR**

Common Mode Gain:

\[
\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} = A_{v,CM} = \frac{-R_D/2}{1/(2g_m) + R_{ss}}
\]

- **Rss** is impedance of current source

- **Good Common Mode Noise Rejection**
Differential Loads

Converts output current into voltage

- Differential resistance
  \[ r_\Delta = \frac{\partial \Delta V}{\partial \Delta I} \]

- Common Mode resistance
  \[ r_C = \frac{\partial V_C}{\partial I_C} \]
  -ve \( R_\Delta \)
  ➔ Positive feedback
  ➔ Hysteresis

Any load mismatch ➔ Reduction in Common Mode Noise Reduction
(or mode couple \( V_C \rightarrow V_\Delta \))

Transistor loads increase \( C \) and decrease BW

**TABLE 4-5 Impedance of Differential Loads**

<table>
<thead>
<tr>
<th>Load</th>
<th>( r_C )</th>
<th>( r_\Delta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>( R )</td>
<td>( R )</td>
</tr>
<tr>
<td>Current mirror</td>
<td>( 1/g_m )</td>
<td>( 1/\lambda I_1 )</td>
</tr>
<tr>
<td>Cross-coupled</td>
<td>( 1/g_m )</td>
<td>(-1/g_m )</td>
</tr>
<tr>
<td>Infinite impedance</td>
<td>( 1/2g_m )</td>
<td>( \infty )</td>
</tr>
</tbody>
</table>

**FIGURE 4-60. Some Differential Load Circuits**

- (a) Differential Load
- (b) Resistor
- (c) Current Mirror
- (d) Cross Coupled
- (e) Infinite Impedance
Differential Flip-flop

Choose this SCL Latch for high speed, differential, noise rejection

- High power consumption

Design @ transistor level

Bandwidth, $C_{load}$

- Pull up Resistor

Swing $\rightarrow$ Tail current

Swing and $V_{th} \rightarrow V_p$

Design transistors’ $W/L$

Simulation with $C_{load}$, $C_{wire}$

Reduce power dissipation as long as requirements met
RX: A sense-amp based latch

After the receiver, the jitter performance is reset by the receiver side clock. Clean data is recovered from the noisy signal.
Self-Biased Differential RX

Self-biased (Chappell) Receiver

- Current source bias
  - Too high → pull input devices out of saturation
  - Too low → limits output swing
  - Self-bias against temp, process variation

Symmetric Chappell Amplifier

High input range amp
Clocked Differential Amplifiers

See earlier section on differential flip-flops

Integrating Amplifier

- Integrator acts like a low-pass filter rejecting high frequency noise
On-chip Termination

Binary-weighted trim resistors

- Set trim bits through comparison of a reference circuit with an off-chip resistor
  - Bridge circuit for comparison

![Diagram of binary-weighted trim resistors](attachment:image.png)
**FET Resistors**

Can give better predictability than Polysilicon resistors:

**Figure 4-61. FET Resistors**

(a) Triode  (b) Two-Element  (c) Pass-Gate

*(Composite: Diode connected on RHS)*

**Figure 4-62. I-V Characteristic of Two-Element FET Resistor**
ESD Protection

Static electricity caused by human and machine handling of ICs

- Human body model:

![Diagram of human body model with 5μH, 1pF, 1.5kΩ, 100pF, 10pF, and 1000-5000 V labels.]

- Effects of ESD
  - Breakdown of gate oxide (at 7x10^8 V/m)
    - “First breakdown” (not necessarily destructive)
    - 4.9 V for 7 nm thick gate oxide
    - 350 V for 0.5 μm thick field oxide
  - Thermal runaway due to high IDS
    - “second breakdown” (destructive)
  - Avalanche and Zener breakdown in parasitic diode
**ESD Protection Circuits**

Overall structure

- **Primary shunt**
  - Goal: to drain current to neighboring input pad through ESD supply
  - Use parasitic diode, FET (using field oxide) or bipolar transistor

- **R** : Low-pass filter. Can be an L, at expense of increased area
  - Use poly or diffusion resistor

- **Secondary shunt**
  - Goal: Voltage clamping: diode-connected nFET

- **Note**: Adds ~1 pF of capacitance to input
Equalization Schemes

Look at Equalization Schemes from three aspects

- Forward or Backward
- Continuous or Discrete-time
- With feedback or without feedback

Real cases

- TX side equalization
- RX side equalization

Noise Aspects of Equalization
1. Forward or Backward

Forward
- FFE (can be FIR or IIR)
- Feed Forward Equalizer

Backward
- DFE
- (Decision Feedback)
- Depends on O/P
2. “discrete” or “continuous”

**Discrete**
- FIR

**Continuous**
- IIR
2. Example of Continuous Equal
3. *With/without Feedback*

**With feedbacks**
- Including: FFE (see above FIR example), DFE

**Without feedbacks**
- Constant or non-adaptive tap co-efficient
**TX side**

**FFE**
- FIR with feedback from the uplink (feedbacks from RX to TX, usually sent as common-mode signal with data link. This is one of the constrains of FFE at TX side)

**FIR without feedback**
- Delayed taps summered with co-efficiencies
- Co-efficiencies are constant or manually adjusted
- Simple to implement, and usually enough to open RX side eye across T-Line variations
**RX side**

**IIR with non-feedback co-efficient**
- Use differential pair degenerated by RC network (inserting Zeros).
- It is continuous, because it’s delayed by continuous RC while not delayed by times of bit period.
- “Infinite” means continuous delay steps while not infinite taps.

**FFE**
- Same IIR, but co-efficient from feedback (usually LMS).

**DFE**
- Subtract received signal by discrete-time delayed bit with co-efficiencies.
- Co-efficiencies generated from usually LMS.
- Essential to get fine equalization and good BER for bad channels.
- Does not amplify noise is another good aspect.
- Need some input eye opening for Clock Recovery.
Summary Questions

What determines the eye opening requirements at an un-equalized RX?
- Horizontal
- Vertical

What are the advantages of DM circuits of single-sided circuits?

How are terminations matched to the line?
Summary Questions

What are the tradeoffs in DM TX design?

What are the tradeoffs in DM RX design?

What is one method to size the taps in a FFE DSP?