I/O Circuits

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Global Outline
- Interconnect Structures and Models
- Signaling
- Driver & Receiver circuits

References
- Dally & Poulton, Chapters 3, 5, 6, 7, 8
- With acknowledgements to Lei Luo, Leon Leong, Rizwan Bashirullah

Outline
- Driver Circuits
- Receiver Circuits
- On-chip termination
- Equalization DSP alternatives
Drivers

Outline:
- Voltage mode drivers
  - Drive and pre-drive
  - Tri-state
  - Rise time control
  - Self-termination
  - Differential
- Current mode drivers
- Transmitter pre-emphasis

Voltage Mode Drivers

Basic Objectives:
- For Vswing > 0.9 Vdd, Rout < 0.1 Z0
  - Large drive transistors
  - Pre-drive circuit needed
  - Remember ratio’d driver (see CMOS notes)
- Must avoid nFET and pFET being on at same time
  - Otherwise large short circuit current during transition
  - Break before Make circuit
- Reasonable area
- Small di/dt
  - Rise time control
Basic Voltage Drivers

Techniques to prevent short-circuit current:

NAND: $t_r > t_f$
NOR: $t_f > t_r$
Use rise, fall times to prevent $I_{sc}$
(beware of process spread)

<table>
<thead>
<tr>
<th>En</th>
<th>Data</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
<td>z</td>
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<tr>
<td>1</td>
<td>1</td>
<td>z</td>
</tr>
</tbody>
</table>

Reduced tri-state driver:

Same functionality as previous page, with fewer transistors and break-before-make
Rise Time Control

Goal: Reduce $\frac{di}{dt}$ without significant reduction in delay
- Typically $t_r < 0.3 – 0.5 \ t_{\text{bit}}$
- Process, temperature variations $\Rightarrow$ Active control might be desirable (e.g. Use nMOS as pFET and control “resistance”)
- First stage to switch usually the largest

Output Impedance Control

- To precisely match line in series termination
- Digitally trimmed circuit
- NC1, NC2, PC1, PC2 produced by comparing copies of the drive FETs with an off-chip resistor (e.g. voltage division or a bridge)
**Current Mode Drivers**

Single sided:
- Relies on saturated FET

![Single sided FET diagram](image)

Requires:
- $V_{out} > V_{DD} - V_{t}$
- Digital trimming to provide $I_{out}$ across process and temp spreads

**Switched Current Mirror**
- Series devices must be large
- Small $V_G$ on mirror to max $V_{sw}$

![Switched Current Mirror diagram](image)

**Gated Current Mirror**
- Smaller devices
- Slower transient response

**Bipolar Current Mode TX**

Above Unipolar
- Levels: 0 and $x$ mA

Create bipolar with complementary pull-up of above
- Logic levels = $+/- x$ mA

Example:

![Bipolar Current Mode TX diagram](image)
Differential Current Mode TX

Current Steering Circuits:
- Stage 1: Converts large swing to small swing
  - Eliminates dead band at ends of swing in stage 2
  - Output starts to swing as soon as $g$ and $g'$ change
- Second stage loaded with line impedance
  - Often $R_{load}$ put in parallel to provide source termination

Large Swing Differential Ckts

Design Issues:
- Output Swing
- Input Swing
- Bandwidth
- Source Matching
- Design of constant current sources
- Resistor Design

Can also be used for high speed differential logic (AND, OR, XOR):
**Current Mirror**

First order treatment

- **M1:**
  - $V_D = V_{GS} \Rightarrow$ Sat
  - $I_{ref} = I_{DS} = \frac{k}{2} \frac{W}{L} (V_{GS} - V_T)^2$

- **M2, M3:**
  - As long as $V_D$ large enough to put into saturation
  - $V_{GS2} = V_{GS3} = V_{GS1}$

  If $L_1 = L_2 = L_3$, then

  \[
  \frac{I_2}{I_{ref}} = \frac{W_2}{W_1} \quad \frac{I_3}{I_{ref}} = \frac{W_3}{W_1}
  \]

- With Channel length modulation taken into account,

  \[
  \frac{I_2}{I_{ref}} = \frac{W_2 / L_2}{W_1 / L_1} \left[ 1 + \lambda V_{DS2} \right]
  \]

Long L1, L2 improves matching

---

**…Current Mirrors**

**FIGURE 4-54. Current Mirrors**

(a) m1 diode connected & in saturation. When m2 in saturation

\[
I_2 = \beta (V_{GG} - V_m)^2 (1 + \lambda V_o) = I_1 (1 + \lambda V_o)
\]

- Make transistors long to reduce $\lambda$.
- Add low pass filter to reduce CM noise from power/ground
- Note: Min voltage drop required over $V_o$ to keep m2 in saturation
Large Swing Differential Drivers

Driver: Design for Large Swing at output

DC (Swing) Analysis:
- M0 must remain in Saturation
  - $V_p > V_{tn}$ (in 0.18 um, a 0.25 V margin is typical)
- $I_{D1} + I_{D2} = I_{tail}$

Swing limits at output:
- Determine by when M1 or M2 are off
  - $V_{high} = V_{DD}$
  - $V_{low} = V_{DD} - I_{tail}R$
- Note: M1, M2 must be large enough to support $I_{tail}$
- Tradeoffs:
  - Increased swing requires high $I_{tail}$
  - Increased power consumption
  - $I_{tail}$ limited by requirement: $V_{low} > V_p$ (see above)

Swing, Bandwidth and Power trade-off

OUTPUT impedance:
- $= R$ at output High
- $= R \parallel |R_{M1}$ at output Low
- Requires High $R_{M1}$ to balance output impedance, put M1 and M2 into saturation will be best

Lumped model $\tau=R*C$ at output, $C$ is the load
- High bandwidth means smaller $R$
  - That's smaller output swing
  - Max swing is $V_x=V_{dd}-I_{tail}*R$
- Increase $I_{tail}$ can improve both bandwidth and Swing
  - But burns more power
### Design Example:

**Design specs:**
- Input swing range: 1.16 to 1.8V
- Output swing range: same as above
- One transistor goes off at max swing
- Data rate $S=5G$ and Load $C_L=100\text{fF}$
- $V_{thn}=0.45V\sim0.52V$, use $0.5V$ here
- Overdrive voltage margin=$0.25V$
- Length $(L)$ of $M_0$, 2 to 3 times of $L_{\text{min}}$ to reduce short channel effect

### Design Procedure

#### Edge Rate
- $t_R \approx 2.2 \cdot RC$
- Want $t_R < t_{\text{bit}}$
- $R < 1/(2.2 \cdot SC) = 900 \text{ Ohm}$
- e.g. Chose $R = 800 \text{ Ohm}$

**Tail current:** $I_{\text{tail}} = (1.8-1.16)/R=0.8\text{mA}$

#### $V_p$
- Keep $M_0$ in saturation and make sure $M_1$ and $M_2$ can turn off
- To keep $M_0$ in saturation implies $V_p > V_t$. E.g. $V_p = 0.75 \text{ V}$ gives $0.25 \text{ V}$ of margin
- To turn $M_1$ off, requires $V_p > V_{\text{in-low}} - V_t = 1.16 - 0.5 = 0.66 \text{ V}$
- $V_p >= 0.75 \text{ V}$
... *Design Procedure*

**M0 Sizing**

- W/L to give \( I_{\text{tail}} \) at \( V_{\text{bias}} \)
- Make long to reduce impact of short channel effects

**M1, M2:**
- To give \( V_{\text{out-low}} \) while maintaining \( V_p \) and keeping it and M0 in saturation

---

**Design for larger swing**

You may want large swing for good SNR

But there are two constraints for large swing:

1. At least:
   - \( V_x > V_p \) (swing limit on \( V_x \))
   - But \( V_p \) has to keep M0 in saturation

2. Better if: \( V_x > (V_{\text{DD}} - V_{\text{th}}) \)
   - to make M1 in saturation
     - To minimize \( C_{gd} \) (Miller effect) and maximize \( R_D \) of M1

So, Max swing is

- \( V_{\text{swing}} = 1.55 \text{ V} \)
  - Reaching the limit, usually can’t meet
- \( V_{\text{DD}} - (V_{\text{DD}} - V_{\text{th}}) = 0.5 \text{ V} \)
  - For good performance
- \( (V_{\text{DD}} - \text{Overdrive})/2 = 0.77 \text{ V} \)
  - Suggested typical

Also applies to the other direction of input
Design for smaller swing:

You want small swing for higher bandwidth
- Or less $I_{\text{tail}}$ for low power, smaller $M_0$ size

Constraints:
1. Noise margin, SNR
2. Large $M_1$ and $M_2$ to get a high $V_p$
   - To turn $M_2$ off
   - For example: $V_p > V_x V_{th}$, if $V_x = 1.4V$, then $V_p > 0.9V$
   - Large $M_1$ and $M_2$ is needed to get a $V_p > 0.9V$, this brings more load to previous stage

Another design example: EX2

- $S$ and $C \rightarrow R = 1/(2.5*{S}\cdot{C}) = 800 \text{ ohm}$
- Tail current: $(1.8 - 1.16)/R = 0.8 \text{mA}$
- $V_p > \text{Max (0.25, 0.4 - 0.5)}$
  - Choose $V_p = 0.25V$
- $V_{bias} = V_{th} + 0.25 = 0.75V$
  - Leave 0.25V as overdrive margin
- $V_p$ and $V_{bias} \rightarrow W/L$ of $M_0 = 48.6\mu/0.54\mu$
  - Design $M_0$ to get such a tail current
- $I_{\text{IN high}} = 1.3V$, get $W/L$ of $M_1$ to make sure $V_p$ of 0.25V $\rightarrow W/L = 4.32\mu/0.18\mu$

Design specs example:
- Input swing range: 0.4/0.45 to 1.35/1.3
- Output swing range: 1.8V to 1.16V
- Data rate $S = 5G$ and Load $C_L = 100fF$
- $V_{th} = 0.5V$, $V_{ov} = 0.25V$, $L = 0.54\mu m$ for $M_0$
### Optimization and Verification: EX2

- If bandwidth allowed, choose higher $R_z$:
  - Resulting in more swing
  - Or allowing smaller $I_{tail}$

- If precise $V_{bias}$ and low gnd noise are available → choose smaller overdrive margin $V_p$ to get more swing

- Check if $M1$ and $M2$ at saturation:
  - $IN_{high}-V_{in}=1.35-0.5=0.85 < OUT_{low}$ Yes, it’s good.

- Check if $M1$ or $M2$ is large enough to carry $I_{tail}$ when Input is high:
  - Requires: $(IN_{high}-V_p-V_{th})^2WM1/LM1 > (V_{bias}-V_{th})^2WM0/LM0$
  - Right=$(0.75-0.5)^2*48.6/0.54=5.6$
  - Left=$(1.3-0.25-0.5)^2*4.32/0.18=7.26 > $Left$
  - Left > Right, some margin is left for body effect

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### Easy Scaling

- Why scaling?
  - To drive $N$ times capacitive load or to provide $N$ times bandwidth

- How to scale?
  - $R/N$
  - $M0*N$; $M1*N$; $M2*N$

- Scaling effect
  - $I_{tail}*N$
  - Bandwidth*$N$ or equivalent cap load *$N$

- Why the design can be scaled?
  - Assume IN/OUT swing range the same
  - It’s all about Remaining $V_p$, $I_{tail}*N$, and $R_{out}/N$
Resistor variation

- Resistors vary largely across corners than transistors

- When R increases
  - $V_p$ decreases
  - $I_{tail}$ remains or negligible decrease
  - Output swing increases
  - $I_{tail}$ need to be calibrated to compensate R variations

Resistor variation – cont.

- Assume $R_S$ and $R_L$ will vary at the same direction linearly
- But since $V_{bandgap}$ remains same, $R_S*I_0$ and $R_L*I_2$ will remain constant, as well as output swing
**Pre-Emphasis**

Simple digital z-domain high pass filter

- Must ensure proper voltage swing

E.g. 2-tap FIR

\[ H(z) = a_0 + a_1 z^{-1} \]

\[ r = -a_1 / a_0 \]

\[ H(z) = a_0 (1-r z^{-1}) \]

\[ H(w) = a_0 (1-re^{jw}) \]

\[ |H(\omega)| = a_0 (1+r^2-2r \cos(\omega))^{0.5} \]

\[ H(\omega=0) = |a_0 (1-r)| = a_0 + a_1 \]

\[ H(\omega=\pi) = |a_0 (1+r)| = a_0 - a_1 \]

Boost = \( \frac{a_0 - a_1}{a_0 + a_1} = \frac{1+r}{1-r} \)

HPF if \( a_0 > 0 \), and \( a_1 < 0 \)

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**Current mode signaling in serial link design**

[Diagram of current mode signaling in serial link design]

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**DAC current source**

\[
I_{DAC} = 0 - 15^*I_{bias}
\]

4-bit Equalization Coefficient

**Voltage Mode Pre-emphasis**

Tap weights effectively set by transistor sizes:
- a1 tap smaller transistors than a0 tap
Tap Sizing

First order design procedure:
If response at end of line to a 010 pulse is:

Then size of taps are \( a_1 \), \( a_2 \) and \( a_3 \) as given above
(i.e. Use taps to subtract this amount from previous “1”s if present).

Receivers

Receivers:
- Basics on detection and sampling
- Inverters
- Differential
- Clocked differential receivers
  - Integrating
  - Matched filter
Detection & Sampling

Eye requirements at input to RX:

- To meet requirements to sample and amplify signal in presence of noise, timing skew and jitter

\[ \text{skew+jitter aperture time} = t_{\text{setup}} + t_{\text{hold}} - t_r \]

Rx sensitivity

Rx offset voltage

Why? aperture time = \( t_{\text{setup}} + t_{\text{hold}} - t_r \)

As tsetup, thold measured to 50% points, aperture at top & bottom of eye (at 10%, 90% points)

Detection and Sampling

UI = Unit Interval (bit period)

- Horizontal eye opening specified in UI
  - Typical requirement ~ 0.7 – 0.8 UI
- Templates often used in standards against eye diagram
Detection & Sampling

Alternatives
- Separate amplifier + sampler (i.e. Flip-flop)
- Clocked amplifier (integrated)

- Advantages of clocked amplifier
  - Lower power
  - Jitter contribution of amplifier “portion” reduced
  - More sensitivity
  - Sampling rate not constrained by gain-bandwidth product

Static (separate) Amplifiers

Inverters
- Gain around $V_{in} \approx 4/((V_{GS}-V_{th})(\lambda p+\lambda n))$
- Gain $\approx 20$ for “book” 0.35 µm process
- Sensitivity $\approx (V_{IH}-V_{IL})/\text{Gain} = 2.5/20 = 125$ mV
- Offset determined variation in $V_{in}$ with process, temp and $V_{dd}$ variations
  - About 300 mV for process variation
  - About 500 mV including temp & $V_{dd}$ variation
- Not best used for initial gain stage in RX
- Useful for final gain stage, however

Inverter Variation
- Schmidt Trigger
  - Hysteresis $\Rightarrow$ very wide NM
Static Differential Receivers

Advantages:
- More sensitive
  - Determined by gm of source coupled pair and RA of load
  - 20 – 100 mV
- Less input offset voltage
  - Determined by nFET, pFET mismatch
  - 10 mV
  - Can be compensated by trim transistors
- Rejects common mode noise at input (i.e. can reject part of received SSN and crosstalk)

Differential Rx

Design Issues:
- Differential voltage gain
  \[ A_d = \frac{V_{out,P} - V_{out,N}}{V_{in,P} - V_{in,N}} \]
- Output swing
- Common Mode Rejection Ratio
  \[ CMRR = \frac{A_d}{A_c} \]
  CM gain: \[ A_c = \frac{V_{out,P} + V_{out,N}}{V_{in,P} + V_{in,N}} \]
- Bandwidth
**Max Swing and Differential Gain**

Maximum Swing (on one side)

\[ \text{Ibias} \times R \] (as before)

Differential gain:

Using Small Swing equivalent circuit

\[ |A_v| = g_m (R) \left| \frac{1}{g_{ds}} \right| \]

Assuming IV square law relationship (first order equations)

\[ \frac{\Delta I_D}{\Delta V_{in}} = A_{I,DM} = \sqrt{\beta I_{SS} R} \]

\[ A_v = A_i R \]

Note: Gain/BW tradeoff, since both increase with R

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**CMRR**

Common Mode Gain:

\[ \frac{\Delta V_{out}}{\Delta V_{in}} = A_{v,CM} = \frac{-R_D}{2} \frac{1}{1/(2g_m) + R_{ss}} \]

- Rss is impedance of current source
- **Good Common Mode Noise Rejection**
Differential Loads

Converts output current into voltage

- Differential resistance
  \[ r_\Delta = \frac{\partial \Delta V}{\partial \Delta I} \]

- Common Mode resistance
  \[ r_C = \frac{\partial V_C}{\partial I_C} \]

Any load mismatch
  ⇒ Reduction in Common Mode Noise Reduction
  (or mode couple \( V_C \rightarrow V_\Delta \))

Transistor loads increase \( C \) and decrease BW

Any load mismatch

Positive feedback

Hysteresis

### Table 4-5: Impedance of Differential Loads

<table>
<thead>
<tr>
<th>Load</th>
<th>( r_C )</th>
<th>( r_\Delta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>( R )</td>
<td>( R )</td>
</tr>
<tr>
<td>Current mirror</td>
<td>( 1/\beta m )</td>
<td>( 1/\beta I_1 )</td>
</tr>
<tr>
<td>Cross-coupled</td>
<td>( 1/\beta m )</td>
<td>( -1/\beta m )</td>
</tr>
<tr>
<td>Infinite impedance</td>
<td>( 1/\beta z_m )</td>
<td>( \infty )</td>
</tr>
</tbody>
</table>

**Differential Flip-flop**

Choose this SCL Latch for high speed, differential, noise rejection

- High power consumption

**Design @ transistor level**

Bandwidth, \( C_{load} \)

⇒ Pull up Resistor

Swing ⇒ Tail current

Swing and \( V_{th} \) ⇒ \( V_p \)

Design transistors’ \( W/L \)

Simulation with \( C_{load} \), \( C_{wire} \)

Reduce power dissipation as long as requirements met
RX: A sense-amp based latch

After the receiver, the jitter performance is reset by the receiver side clock. Clean data is recovered from the noisy signal.

Self-Biased Differential RX

Self-biased (Chappell) Receiver
- Current source bias
  - Too high → pull input devices out of saturation
  - Too low → limits output swing
  - Self-bias against temp, process variation

Symmetric Chappell Amplifier

High input range amp
**Clocked Differential Amplifiers**

See earlier section on differential flip-flops

**Integrating Amplifier**
- Integrator acts like a low-pass filter rejecting high frequency noise

![Integrator Diagram](image)

**On-chip Termination**

Binary-weighted trim resistors
- Set trim bits through comparison of a reference circuit with an off-chip resistor
  - Bridge circuit for comparison

![On-chip Termination Diagram](image)
**FET Resistors**

Can give better predictability than Polysilicon resistors:

![FET Resistors Diagram](image)

**ESD Protection**

Static electricity caused by human and machine handling of ICs

- Human body model:

![Human Body Model Diagram](image)

- Effects of ESD
  - Breakdown of gate oxide (at 7x10^8 V/m)
    - “First breakdown” (not necessarily destructive)
    - 4.9 V for 7 nm thick gate oxide
    - 350 V for 0.5 μm thick field oxide
  - Thermal runaway due to high IDS
    - “second breakdown” (destructive)
  - Avalanche and Zener breakdown in parasitic diode
**ESD Protection Circuits**

**Overall structure**

- **Primary shunt**
  - Goal: to drain current to neighboring input pad through ESD supply
  - Use parasitic diode, FET (using field oxide) or bipolar transistor
- **R**: Low-pass filter. Can be an L, at expense of increased area
  - Use poly or diffusion resistor
- **Secondary shunt**
  - Goal: Voltage clamping: diode-connected nFET
- **Note**: Adds ~1 pF of capacitance to input

**Equalization Schemes**

Look at Equalization Schemes from three aspects

- Forward or Backward
- Continuous or Discrete-time
- With feedback or without feedback

**Real cases**

- TX side equalization
- RX side equalization

**Noise Aspects of Equalization**
1. Forward or Backward

**Forward**
- FFE (can be FIR or IIR)
- Feed Forward Equalizer

**Backward**
- DFE
- (Decision Feedback)
- Depends on O/P

2. “discrete” or “continuous”

**Discrete**
- FIR

**Continuous**
- IIR
2. Example of Continuous Equal

Example of Continuous

\[
\begin{align*}
\text{OUT}_N & \quad \rightarrow & \quad \text{OUT}_P \\
\text{IN}_P & \quad \rightarrow & \quad \text{IN}_N
\end{align*}
\]

3. With/without Feedback

With feedbacks
- Including: FFE (see above FIR example), DFE

Without feedbacks
- Constant or non-adaptive tap co-efficient

\[
\begin{align*}
\text{FIR} & \\
\text{CO} & \rightarrow \text{C1} \rightarrow \text{C2} \rightarrow \text{C3}
\end{align*}
\]

Least Mean Square Optimizer
**TX side**

**FFE**
- FIR with feedback from the uplink (feedbacks from RX to TX, usually sent as common-mode signal with data link. This is one of the constrains of FFE at TX side)

**FIR without feedback**
- Delayed taps summered with co-efficiencies
- Co-efficiencies are constant or manually adjusted
- Simple to implement, and usually enough to open RX side eye across T-Line variations

**RX side**

**IIR with non-feedback co-efficient**
- Use differential pair degenerated by RC network (inserting Zeros).
- It is continuous, because it's delayed by continuous RC while not delayed by times of bit period
- “Infinite” means continuous delay steps while not infinite taps

**FFE**
- Same IIR, but co-efficient from feedback (usually LMS)

**DFE**
- Subtract received signal by discrete-time delayed bit with co-efficiencies.
- Co-efficiencies generated from usually LMS.
- Essential to get fine equalization and good BER for bad channels.
- Does not amplify noise is another good aspect.
- Need some input eye opening for Clock Recovery
Summary Questions

What determines the eye opening requirements at an un-equalized RX?
- Horizontal
- Vertical

What are the advantages of DM circuits of single-sided circuits?

How are terminations matched to the line?

What are the tradeoffs in DM TX design?

What are the tradeoffs in DM RX design?

What is one method to size the taps in a FFE DSP?