Logic Design – Final Thoughts

Dr. Paul D. Franzon

Outline
1. Reminder – transistor sizing basics
2. Logical Effort
3. LSDL

References
• Sutherland, Sproull, Harris, “Logical Effort”
Transistor Sizing

Key Steps:

- Simplify circuit as RC equivalent
- Consider RC delay from when transistor turns on
- Make sure to include any effects of delay opposing transistor turn-off

\[ x, y \rightarrow 1,1 \]

\[ x, y \rightarrow 0,1 \]
Logical Effort

Assuming an RC model, what is the delay of this gate?

\[ \text{Delay} \propto R_1.C_{\text{inv}} + R_1.C_{\text{pinv}} \]

Cp-inv: Drain/Source parasitic

How does \( R_1.C_{\text{pinv}} \) vary with scale factor \( x \)?

How does \( R_1.C_{\text{inv}}^2 \) vary with \( x \) and \( y \)?

\[ \text{Delay} \propto g.h + p \]

\[ g = \text{“logical effort” (=1 for INV) (gate type)} \]
\[ h = \text{“electrical effort” = y/x (transistor widths)} \]
\[ p = \text{gate parasitic delay} \]
... Logical Effort

If drive gate is a NOR gate, how do you modify \( g \) so that \( h \) preserves its meaning on the previous page?

What transistor sizes would you have to make gate have same drive strength as INV?
  - See RHS

What is the ratio of \( \text{Cin} \text{(NOR)} \) to \( \text{Cin} \text{(INV)} \)?

How much would \( R_1 \) increase by to make \( \text{Cin} \text{(NOR)} = \text{Cin} \text{(INV)} \)?

What is \( g \) for a 2-input NOR gate?

\[
\text{Delay} \propto g.h + p
\]
**Logical Effort**

Values for g and typical values for p:

<table>
<thead>
<tr>
<th>g</th>
<th>2-input</th>
<th>3-input</th>
<th>4-input</th>
<th>p</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAND</td>
<td>4/3</td>
<td>5/3</td>
<td>6/3</td>
<td>npinv</td>
</tr>
<tr>
<td>NOR</td>
<td>5/3</td>
<td>7/3</td>
<td>9/3</td>
<td>npinv</td>
</tr>
<tr>
<td>MUX</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2npinv</td>
</tr>
<tr>
<td>XOR</td>
<td>4</td>
<td>12</td>
<td>32</td>
<td>4npinv</td>
</tr>
</tbody>
</table>

Gate Delay

\[ d = (gh + p) \tau \]

\[ f = gh \text{ called } \textit{effort delay of gate} \]
Logical Effort for Multistage Logic

Path Effort

\[ F = GBH \]
\[ G = \Pi g_i \text{ for gates along the path} \]
\[ H = \text{Cout}/\text{Cin} \text{ for path Out & In} \]
\[ B = \Pi b_i \text{ for nodes along path (accounts for fanout)} \]
\[ b_i = \text{Cotal}/\text{Con-path at each node in path} \]

The path delay for an N-stage network is least when the path delay for each stage is the same. i.e. when \( f = F^{1/N} \) or slightly larger
(For proof see Sutherland, but consider case of ratioed buffer chain)
Then for each stage the optimum electrical effort is \( h = F^{1/N}/g \)

Delay Effort

\[ D = \Sigma g_i h_i + \Sigma p_i \]
Consider alternatives:

A:

\[
\begin{align*}
g &= 2 \\
p &= 4 \\
b &= 1 \\
G &= 3.33
\end{align*}
\]

B:

\[
\begin{align*}
g &= \frac{5}{3} \\
p &= 2 \\
b &= 1 \\
G &= 2.96
\end{align*}
\]

Optimum Delay when \( f = (GBH)^{1/N} \)

A: Optimum Delay \( D = 2 \left( \frac{3.33H}{2} \right)^{1/2} + 6 \)

B: Optimum Delay \( D = 4 \left( \frac{2.96H}{4} \right)^{1/4} + 7 \)

e.g. \( H = 1 \):

Case A delay = 9.6

Case B delay = 12.7

e.g. \( H = 12 \):

Case A delay = 18.6

Case B delay = 16.8
**Example**

**Gate Sizing**

H = 12 case

If Cin = 4

then Cout = H Cin = 48

Optimal Stage Effort = \( F^{1/4} = (2.96H)^{1/4} = 2.44 \)

Each stage \( h = \frac{Cout}{Cin} = \frac{F^{1/N}}{g} \)

\( \Rightarrow Cin = Cout g / (F^{1/N}) \)

INV: \( Cin = 48 / 2.44 = 19.66 \)

Next NAND: \( Cin = 19.66 \times (4/3) / 2.44 = 10.73 \)

Etc. Decides relative gate sizes