Memories

Dr. Paul D. Franzon

Outline
• DRAM
• SRAM
• Flash memory
• Emerging Memories

References
• Kang & Leblecici, CH 10

1©2006, Dr. Paul D. Franzon, www.ece.ncsu.edu/erl/faculty/paulf.html

2©2006, Dr. Paul D. Franzon, www.ece.ncsu.edu/erl/faculty/paulf.html
Read Operation

Why is PSIO “overboosted” to Vpp > Vdd?

What is the swing on BL at time A?

What happens at time B?

What happens at time C?

What happens at time D?
**Write Operation**

*Same as Read*

BL/BLB

CS

BL_IO/BL_IOB

*BL_IO/B overcomes latch in sense-amp*

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**SRAM Cell**

*Column Pull Up transistors*

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Read

Basic Operation:

- M1 pulls BL down slowly
- Drop amplified by sense amp
- Retains data as long as M2 and M5 stay off

How to keep M2 off?

- Requires: \( V_{GS2} < \)
- \( V_{GS2} = V_{DS1} \)
- States
  - M1:
  - M3:
- Equating \( I_{DS1} = I_{DS3} \) permits solution of constraint above that keeps M2 off
- Solution requires M1 be larger than M3

Write

Due to the read constraint, \( V_{GS1} \) cannot be brought high enough to turn M1 on

- Instead size transistors so M2 is turned off
  - \( V_{GS2} < V_t \) (*)
  - Then \( V_{GS2} \) will rise
- Some time after BL brought low M3 will become linear and M5 will go into saturation
  - Equate \( I_{DS3} = I_{DS_5} \)
  - For for (*) will give M5 will have to be sufficiently smaller than M3
SRAM Sense Amp - Read

Current Mode Amplifier (transistors in saturation)
nFET in cell becomes a small current source which gets amplified by this current diff-amp

Flash Memory
Charge stored on floating gate changes Vt

Programming through hot electron injection:
- High lateral field
  - Avalanche breakdown generates hole/electron pairs. Electrons injected into floating gate via high gate field

Program via tunneling:
- Apply high Vpp to D or S
- Electrons tunnel

Control gate
Gate oxide
Floating gate
Tunneling oxide (10 nm)

n+ p substrate

Vg>Vdd
0
Vpp>Vdd
0

Vdd
Vdd

Hot electron
Tunneling
Flash Memory Operation

Changing charge stored on floating gate changes $V_t$:

$$\Delta V_T = \frac{\Delta Q}{C_{FG-CG}}$$

- $V_R$ enough to turn “0” gate on but “1” gate off

NOR Flash RAM

Program:
- Hot electron
- $BL=1$ V; $WL=12$ V; $SL=0$ V;

Erase:
- Tunneling
- $BL=open$; $WL=0$ V; $SL=12$ V;

Read:
- $BL=1$ V; $WL=5$ V; $SL=0$ V
- Gives $IDS > 0$ if “0” stored

Not Read:
- $BL$ and/or $WL=0$ V

Need current amplifier for sense amp
**NAND Flash RAM**

Program:
- Tunneling
- BL=0V; WL = 20 V; SL = 5 V; source Line = 0
- Other WL = 10 V

Erase:
- Tunneling
- BL=0V; WL = 0 V; SL = 5 V; source Line = open; pwell = 20 V
- Other WL = 10 V

Read
- 0V applied to selected WL; 5 V to other
- Will complete pull down path if 0 stored

Smaller; slower and less scalable than NOR flash structure

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**Emerging Memory technologies**

Magnetorestrictive RAM (MRAM)
- Magnetic tunnel junction (MTJ) can change conductance state based on history of H field
- Read by comparing on resistance with a reference resistance

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### Comparison

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>MRAM</th>
<th>FLASH</th>
<th>SRAM</th>
<th>DRAM</th>
<th>FeRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density 90nm</td>
<td>256kb-1Mb</td>
<td>1Mb-32Mb</td>
<td>4Mb-256Mb</td>
<td>4Mb-64Mb</td>
<td>4Mb-64Mb</td>
</tr>
<tr>
<td>Density 90nm</td>
<td>256kb-1Mb</td>
<td>1Mb-32Mb</td>
<td>4Mb-256Mb</td>
<td>4Mb-64Mb</td>
<td>4Mb-64Mb</td>
</tr>
<tr>
<td>Wafer Size (mm)</td>
<td>150/200</td>
<td>200</td>
<td>200/300</td>
<td>200/300</td>
<td>200/300</td>
</tr>
<tr>
<td>Performance (MHz)</td>
<td>16</td>
<td>50-100</td>
<td>75-125</td>
<td>20-100 Read</td>
<td>50-200</td>
</tr>
<tr>
<td>Array Efficiency</td>
<td>40%-60%</td>
<td>40%-60%</td>
<td>40%-60%</td>
<td>25%-40%</td>
<td>50%-80%</td>
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<tr>
<td>Voltage</td>
<td>3.3</td>
<td>3.3/1.8</td>
<td>2.5/1.2</td>
<td>2.5/1.2, 5-12 internal</td>
<td>2.5/1.2</td>
</tr>
<tr>
<td>Non-Volatility</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
</tbody>
</table>

**Magnetoresistive random access memory using magnetic tunnel junctions**


Proceedings of the IEEE

Volume 91, Issue 5, May 2003 Page(s):703 - 714

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### Phase change Memory

**Material changes resistance when heated by electric current**

Current status of the phase change memory and its future

**Carbon Nanotube Memory**

**Nano-mechanical relay**

A nonvolatile nanoelectromechanical memory element utilizing a fabric of carbon nanotubes

Non-Volatile Memory Technology Symposium, 2004

**Nanocrystal Flash**

Replace floating gate with one or more nanoparticles

- Increase capacitance and allow smaller overall areas

**Metal Nanocrystal Memory With High-kappa5 Tunneling Barrier for Improved Data Retention**

Lee, J.J.; Kwong, D.-L.;
Electron Devices, IEEE Transactions on
Volume 52, Issue 4, April 2005 Page(s):507 - 511
Summary

What type of sense amp is used in DRAMs?

What type of sense amp is used in high speed SRAMs?

What considerations are used to size SRAM transistors?

What is the operational principle of FlashRAMs?