Signaling

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Global Outline
- Interconnect Structures and Models
- Signaling
- Driver & Receiver circuits

References
- Dally & Poulton, Chapters 3, 5, 6, 7, 8

Outline

Signaling
- Goals
- Noise Evaluation
  - Eye Diagrams
  - ISI and channel equalization
- Basic Approaches
  - Timing Approaches
  - Voltage vs. Current Mode
  - Single Side vs. Differential
- Coding
  - Run-length codes
  - Symbol codes

References
- Ch. 7,8 D&P
Goals

Transmit data at required bit rate
- At a low Bit Error Rate (BER)
  - BER = $10^{-15}$ for older systems; $10^{-18}$ or $10^{-21}$ for future systems
  - BER limited by
    - Clock jitter (phase noise)
    - Aperture for signal capture
    - Noise Margin (voltage noise)
- At low power consumption

Problems and Issues
- Common mode noise on power & ground
- Reflection and Crosstalk Noise
- Clock strategies
- Channel and channel compensation

Bit Error Rate

Best determined through experimentation
- Apply pseudo-random test pattern
- Measure logical output for bit value errors
- Requires full $2^{N-1}$ patterns to be effective
  - One worst case pattern is possible

Can be evaluated via eye diagram
- Only suitable technique at lower BERs
- E.g. At 3 Gbps, establishing a BER of less than $10^{-12}$ requires 6 minutes of error-free operation, while establishing a BER of less than $10^{-18}$, requires 10 years
Eye Diagram Analysis

Procedure:
- Captures InterSymbol Interference (ISI)
  - “leftover” noise from previous bits
- Plot random sample of waveforms on top of each other
  - Make sure eyes are ‘well open’ (>40%)
- Ensure clock ‘envelope’ well within data ‘envelope’

RMS Jitter = \( \sigma_t \)
- Jitter in both signal and clock in practice!
  - (signal jitter included in -max values)

Bit Error Rate (BER)
- Related to Q Factor
  - Q factor = \( \frac{(P_1-P_0)}{(\sigma_1-\sigma_0)} \)
  - For evaluation only – not true BER!

\[
\text{BER} = \frac{1}{2} \text{erfc} \left( \frac{Q}{\sqrt{2}} \right) = \frac{\exp(-Q^2 / 2)}{Q \sqrt{2\pi}}
\]

Sample:

<table>
<thead>
<tr>
<th>Q</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>-10^{-9}</td>
</tr>
<tr>
<td>7</td>
<td>-10^{-12}</td>
</tr>
</tbody>
</table>

Constructing an Eye Diagram

Simulate data and clock for different process variations, different temperatures, different data patterns, etc.
- Full path simulation, including package, connectors, vias, etc.
- Make sure to include clock skew and jitter

\( V_{IL} \)
\( V_{IH} \)

Clock Jitter

Open Eye

Intersymbol Interference

Duration delay
\( t_{\text{setup}} \)
\( t_{\text{hold}} \)
Estimate BER by EYE

Note: Here we assume the signal is gauss distributed.

BER is expressed here by the shadow area:

Blue shadow for BER of ‘1’
Red shadow for BER of ‘0’

BER=Integration of the shadow area

\[
BER = \int_{-\infty}^{\infty} \frac{1}{\sigma_t \sqrt{2\pi}} \exp\left(-\frac{x^2}{2\sigma_t^2}\right)dx + \int_{-\infty}^{\infty} \frac{1}{\sigma_0 \sqrt{2\pi}} \exp\left(-\frac{x^2}{2\sigma_0^2}\right)dx
\]

\[
= \frac{1}{2} \text{erfc}\left(\frac{NMH}{\sqrt{2}\sigma_t}\right) + \frac{1}{2} \text{erfc}\left(\frac{NML}{\sqrt{2}\sigma_0}\right)
\]

if \( \sigma_0 = \sigma_t = \sigma \), \( NMH = NML = 0.6V \),

\[
BER = \text{erfc}\left(\frac{NM}{\sqrt{2}\sigma}\right) \leq 10^{-12} \iff \sigma = \frac{NM}{7} \leq 0.085V
\]

\[
BER = \text{erfc}\left(\frac{NM}{\sqrt{2}\sigma}\right) \leq 10^{-17} \iff \sigma = \frac{NM}{8.6} \leq 0.07V
\]

How to find \( \sigma \)?

Note: Here we assume the signal is gauss distributed.
Eye Diagram

Can obtain from Channel Impulse Response:

Measurement technique (TDR & TDT):

- Step Response
- SMA Card Connector Backplane

Differentiate Step Response

Impulse response here

- [1-2] : 0.4 ns
- [1-2-1-5] : 0.8 ns
- [3-4] : 4.2 ns
- [3-5] : 4.4 ns

Construct from Step Response

Pulse response = +step followed by - step

Eyes for 101010
**Eye Diagram**

**ISI Accumulation:**

Eye for random data with maximum run length of 7.

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**Effect of Channel Equalization**

3-Ways to Look at Equalization:

- Sharpen the Step Response
- Remove the Tail of the Pulse Response
- Flatten the Frequency Response to Nyquist
**Bit Error Rate Estimation**

ISI Accumulation from Pulse Response

Pulse tail at time bit count @ interval

**ISI**

Frequency-dependent attenuation in Channel produces inter-symbol interference (ISI):

Lone 1 in stream of 0's undetectable

Equalization required when attenuation more than a few dB per octave
Crosstalk.

Max bit rate may be limited by crosstalk, rather than channel attenuation

\[ \frac{S_{21}}{\Sigma(x_{\text{Talk}})} \]

Frequency

Signal to crosstalk margin

Synchronous Design

- Synchronize Asynchronous signals ASAP
  - Put through several flip-flops in sequence
  - Use active low control signals (e.g. Reset)
    - As \( \text{NM}_H > \text{NM}_L \)

- Overshoot matters (porches on rising edge can matter too)

Can:
- Reprogram logic
- Turn on parasitic diodes
- Reduce long term reliability
  - (injected gate current)
Design Alternatives

Timing Scenarios (Clocking strategy)
- Master synchronized clock
- Source synchronous clocking
- Clock Recovery

Basis for Signaling Circuit
- Voltage Mode vs. Current Mode
- Single sided vs. Single sided against reference vs. Differential

Termination
- Source vs. Load vs. On-chip

Direction
- Single direction vs. Bidirectional

Data Representation
- Non Return to Zero vs. Return to Zero vs. Pulse vs. N of M Code (e.g. 8b/10b)
- Pulse Amplitude Modulation: PAM-2 (binary) vs. PAM-4 (4-level)

Use of Channel Compensation
Use of Error Correcting Codes

Timing Scenarios

- Sufficient delay slack for noise to settle:

  ![Diagram of timing scenario]

  - If \( t_{\text{intconnect-max}} < 5 \times \text{line delay} \), then design is very simple.

- First Incident Switching:

  ![Diagram of first incident switching]

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...Timing Scenarios

Source-Synchronous Switching

- Send clock with data
  - (or recover clock from data)

- In such systems, the rise-times and skew from inter-symbol noise, processing and temperature variations determines maximum signal speeds

  E.g. 2 Gbps, 30 inch wire
  \[ t_{\text{symbol}} = 500 \text{ ps} \]
  \[ t_{\text{wire}} = 5 \text{ ns} \]

  If clock jitter has to be less than 10% of \( t_{\text{symbol}} \), \( t_{\text{jitter}} = 50 \text{ ps} \)
  What % variation in clock “t_wire” would be acceptable? 1%
  If a via \( C_L = 1 \text{ pF} \), \( Z_0 = 50 \text{ Ohm} \), what is the \( \tau \) of a via? 50 ps

  Meeting such timing constraints over long distances is very hard.

Clock & Data Recovery

- Recover clock from the data so that delay does not need to be precisely controlled.

- Issues:
  - Ensuring enough edges in data signal to generate clock
  - Design of clock recovery circuit (Phase Locked Loop, Delay Locked Loop)
Voltage Mode Signalling

- RX sensitivity 300 mV
  - $V_{out} = A \cdot V_{in}$ enough to provide full swing at O/P
- Energy per transition, $E_{sw} = \Delta V^2 t_{line} / Z_0 = \Delta I^2 t_{line} Z_0$

Comparison: (Ignore lines losses)
- Voltage Mode, Series Termination
- Voltage Mode, Parallel Termination

Current Mode Signalling

- RX sensitivity 300 mV
  - $V_{out} = A \cdot V_{in}$ enough to provide full swing at O/P
- Energy per transition, $E_{sw} = \Delta I^2 t_{line} / Z_0 = \Delta I^4 t_{line} Z_0$

Comparison: (Ignore lines losses)
- Current Mode, Parallel Termination
Single sided vs. Differential

Cost:
- Full differential doubles board real-estate, and pin-count

Performance

<table>
<thead>
<tr>
<th>Single sided</th>
<th>Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Single sided diagram" /></td>
<td><img src="image2" alt="Differential diagram" /></td>
</tr>
</tbody>
</table>

Sensitivity: Smallest RX input to give full swing at output (limited by gain A)

Noise:
TX:
- TX transmits substantial portion of power/gnd noise as CM noise
- TX has low CM gain

RX:
- Amplifies noise at input as normal
- Noise on Tran line behaves as differential noise
- Rejects CM noise on input signal

Termination

Parallel vs. Series
- See above

Off-chip vs. On-chip
- High-speed requires on-chip

![Package diagram](image3) Package (~100 ps delay) ![Rterm diagram](image4) No additional reflection noise due to package delay

- How?
  - Common approach: Use transistors and trim against an off-chip resistance comparison
**BiDirectional Signalling**

Halves number of wires and pins!

**Current Mode:**

![Diagram of BiDirectional Signalling](Reference return for T line)

- Estimates V\text{transmit} from TX and subtracts it from signal at pin
- Speed limited compared with single sided as estimate is imperfect (due to package, R\text{term} mismatch, etc.) and ISI tends to be larger
- Voltage mode and differential versions

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**Signal Coding**

- Run length constrained and DC balanced codes
- Error Correction Coding
  - Not used much today but possible in future
  - Pulse Amplitude Modulation (PAM), NRZ vs. RZ

Reasons to constrain max # and ratio of 1’s or 0’s

- AC Coupled Signals

![AC Coupled Signals Diagram](Vbias)  

- Provide sufficient edges for clock recovery
  - Max # of 1’s or 0’s in sequence known
- Reduce SSN, return current and \(\frac{d}{dt}\)(return current)
  - Balance 01 and 10 simultaneous transitions in a bus

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Concepts in Balanced Codes

Run Length
- Max # of 1’s in sequence = r_max
- Min # of 1’s in sequence = r_min
- Code referred to as (r_min-1, r_max-1) code

Bit Stuffing
- Simplest way to achieve a (0,m) code is to insert a false bit when r_max hit
- Requires synchronization at frame level and counters at RX and TX
- E.g. Achieving (0,2)
  - Data: 010001110
  - Encoded data: 010001011100
- Though reduces low frequency content, does not eliminate a DC bias drift
- Can not predict actual symbol rate
  - Can predict worst case symbol rate
    - What is it for (0,2)?

Disparity
- \( \text{Disparity} = \# \text{ of 1's} - \# \text{ of 0's} \)

Digital-Sum Variation (DSV)
- \( \text{DSV} = \text{Max. variation in disparity} \)
- Constant DSV \( \Rightarrow \) DC-balanced signal, \( r_{\text{max}} = \text{DSV} \)
- Determines low frequency components of signal

E.g. 8B10B code
- 8-bit Data Bytes encoded as 10-bit characters
- 12 control characters are encoded too
- Run length of 5
- DSV = 3
**Block Codes**

**Nonoverlapping Block Codes**
- Each block of $n$ bits is coded as $m$ bits with equal numbers of 1s and 0s.
- Number of zero-disparity code words in $m$ bits is $\binom{m}{n/2}$.
- Number of input signals is $2^n$.
- Thus code exists if $\binom{m}{n/2} > 2^n$.
- Code efficiency $= n/m$.
- E.g. $n=2$, $m=4$.
- E.g. $n=8$, $m=12$, efficiency $= 67\%$.

<table>
<thead>
<tr>
<th>input</th>
<th>code</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0101</td>
<td>50%</td>
</tr>
<tr>
<td>01</td>
<td>1010</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>1100</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>0011</td>
<td></td>
</tr>
</tbody>
</table>

**Running Disparity Codes**
- Permits non-zero disparity in “code word”.
- Constrains worst case disparity.
- Disparity = disparity of current block.
- Accum = accumulated disparity, including comp bit.
- Compare = 1 if Disparity and Accum have same signs.
  $= \neg\text{sign(accum)}$ if disparity $= 0$.
- Max run length $= 2(n+1)$; Disparity ranges over $[-3n/2, 3n/2]$.
- DSV $= 3n$.
- 8-bit burst error occurs whenever comp bit wrong.
**Spatial N of M Signalling**

Used to reduce Common Mode noise in power/ground/return system
- Reduces SSN at TX
- Reduces signal return current
- e.g. Hamming Codes

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**Single Symbol Encoding**

NRZ = Non Return to Zero
RZ = Return to Zero
Ternary = 3 level signaling
PAM-4 = Encode bit pair (symbol) as one of 4 levels

<table>
<thead>
<tr>
<th>Symbol</th>
<th>NRZ</th>
<th>RZ</th>
<th>Ternary NRZ</th>
<th>Ternary RZ</th>
<th>PAM-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>0</td>
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<td>0</td>
<td>1</td>
<td>1</td>
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<td>1</td>
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<td>1</td>
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<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Symbol Encoding Tradeoffs

- NRZ (also called PAM-2)
  - Most common
- RZ
  - Requires 2* channel bandwidth of NRZ
  - (Only used in optical signals where BW is almost infinite)
- Ternary NRZ
  - Use against Vref in single-sided TX, differential RX
- Ternary RZ
  - DC balanced
  - Use against Vref in single-sided TX, differential RX
- PAM-4
  - Requires half channel BW of PAM-2
  - Reduced signal swing per symbol
  - Requires ADC at RX
  - Not useful unless channel BW very limited

Multi-level Signaling

2-PAM (NRZ) signaling simple & robust
  - Operates at lowest BER for given SNR
But, may be difficult or impossible to equalize a “bad” channel sufficiently,
Or, severe crosstalk may use up margin
4-PAM signaling for “bad” channels
  - 2 bits/baud
  - Same bit rate at half the baud rate of 2-PAM
When should you use 4-PAM?

- If attenuation increases by more than 10dB over an octave, 4-PAM should be considered.

4-PAM Cautions

- Eye height 1/3 of 2-PAM, so 10dB less amplitude per bit
- Re-introduces the “reference problem” at the receiver (no reference needed for 2-PAM).
- Edge trajectories close eye horizontally
- 2-PAM / 4-PAM crossover more like 15dB/octave
Summary

What are the main factor(s) that cause eye closure?

How is equalization useful?

How are current mode and voltage mode signalling different?

What are the advantages of single-sided TX, differential RX over single-sided RX?

Inter Symbol Interference (ISI) due to limited edge rate and noise.

Increases Edge Rate by inserting a HPF, reducing ISI and BER

Driving line with $\Delta I$ vs. $\Delta V$

Increased sensitivity of RX

Rejects CM noise on Gnd and Power supply at RX

... Summary

What is the advantage of a full differential system?

What are the uses of DC-balanced and run-length codes?

What is the potential advantage of PAM-4 over PAM-2?