Question 1
This is a straightforward revision question.

Design a static gate that performs F=((A+C).(B+D))’. [10 points]

Question 2
This is a more complex revision question that forces you to think through the operation of a more complex static gate and revisit the first level device equations.

Consider the Schmidt Trigger gate. This is useful at noisy inputs as it provides an improved noise margin.

Obtain approximate expressions for VIL and VIH in terms of kNf, kN1, etc. Use the first order transistor equations and ignore the body effect. Note that normally Nf and Pf are larger than the other transistors. [20 points]

Hint: Estimate VIH by determining the smallest Vin that permits transistor N2 to turn on. Estimate VIL by determining the Vin that turns P2 on, while Vin is rising.

Question 3
The main purpose of this question is to get you to start using Spice and to perform some of the trade-off analyses typical for this class. Please note the following:

- Use the TSMC 0.20 um SUB CMOS018 technology. You will see this referred to as TSMC20 in the NCSU Cadence install. The TSMC 0.18 SUB model files are under /ncsu/cadence/local/models/hspice/public/publicModel tsmc20N and tsmc20P
• I prefer you use Cadence Composer for schematic capture, rather than write a Spice Netlist by hand. That way, I know you have the drain and source areas and perimeters correct. If you are doing the Spice Netlist by hand, make sure to check these figures.
• Make sure to use the power calculation approach outlined on the CAD tool tips (resources) page.

Design a Schmidtt Trigger gate so that NMH = NML within a range of 10%. Make sure the design works in simulation to this specification. When loaded with a minimum size inverter what is the gate delay (use an input waveform with a 0-100% rise time of 100 ps)? Measure the average power consumption over an interval of 5 ns with the following conditions:
• Input: Low for 1 ns. 100 ps rising edge (0 to 100% rise time). High for 2 ns. 100 ps falling edge (100% to 0% fall time).
• Loaded with a CMOS inverter containing minimum size gates. Do not include the power consumption of the CMOS inverter in the power figure.

Report your results, including the schematic and plots of corresponding delay waveforms.