Static Combinational Circuits

Dr. Paul D. Franzon
Outline

1. CMOS Inverter
   - DC and AC characteristics

2. Static logic gates
   - Structure
   - Relative transistor sizing
   - Multi-Vt circuits

3. Differential Cascode Voltage Switch (DCVS) Logic
   - Structure
   - Transistor Sizing

4. Pass Gate Logic
   - Structures & Alternatives
   - Transistor Sizing

References:
Dally & Poulton, Chapters 4, 12.1
# Basic CMOS Circuit Analysis

**Core Principle:**

Analysis of any digital circuit usually revolves around determining the transistor states for each region of operation.

<table>
<thead>
<tr>
<th>Region</th>
<th>State</th>
<th>Equivalent Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>V_{GS}</td>
<td>&lt;</td>
</tr>
<tr>
<td>$</td>
<td>V_{GS}-V_T</td>
<td>&gt; V_{DS} \geq 0$</td>
</tr>
<tr>
<td>$V_{DS} \geq</td>
<td>V_{GS}-V_T</td>
<td>\geq 0$</td>
</tr>
</tbody>
</table>

Source of “majority carriers”
(e- in nmos case, p+ in pmos)
CMOS Inverter

Static CMOS Inverter:

- Transfer Characteristic:

1. $Vin = 0$, $Vout = Vdd$
   - N: $V_{GS}=0$, $V_{DS}=3.3$, $|V_{GS}| < |V_T|$ : Off
   - P: $V_{GS}=3.3$, $V_{DS}=0$, $|V_{GS}-V_T| > V_{DS}$ : LINEAR

2. $Vin > |V_T|$
   - N: $V_{GS} \approx 1$, $V_{DS} \approx 3$, $V_{DS} \geq |V_{GS}-V_T|$ : SATN
   - P: $V_{GS} \approx 3$, $V_{DS} \approx 0.3$, $|V_{GS}-V_T| > V_{DS}$ : LINEAR

3. $Vin \sim Vout$
   - N: $V_{GS} \approx 1.6$, $V_{DS} \approx 1.6$, $V_{DS} \geq |V_{GS}-V_T|$ : SATN
   - P: $V_{GS} \approx 1.6$, $V_{DS} \approx 1.6$, $V_{DS} \geq |V_{GS}-V_T|$ : SATN

4. N: LINEAR; P: SATN
5. N: LINEAR; P: OFF

To simplify, use $V_{dd}=3.3$ V
$|V_T| = 0.5$ V in examples

$V_{DD}+V_{tp}$ $V_{tn}$ $V_{tn}$ $V_{tn}$ $V_{tn}$

$V_{dd}$ $V_{dd}$ $V_{dd}$ $V_{dd}$ $V_{dd}$

3: High Gain Region

Gain = $\frac{4}{((V_{GS}-V_T)(\lambda_p+\lambda_n))}$
**CMOS Inverter**

"Trip" Voltage

- where Vout = 0.5 VDD
  - Both nFET and pFET in saturation

\[ I_{DSn} = -I_{DSP} \]

\[ \frac{\beta_n}{2} (V_{in} - V_{Tn})^2 = -\frac{\beta_p}{2} (V_{in} - V_{DD} - V_{Tp})^2 \]

\[ Vin = \frac{V_{DD} + V_{tp} + V_{in} \sqrt{\beta_n / \beta_p}}{1 + \sqrt{\beta_n / \beta_p}} \]

- If \( \beta_n = \beta_p \) and \( V_{tn} = -V_{tp} \), \( Vin = VDD/2 \)  \( \text{(1.65 V with parameters on prev. page)} \)

- What if \( k_n = 2k_p \), \( W_n/L_n = W_p/L_p \), \( VDD = 3.3 \), \( V_{tn} = -V_{tp} = 0.5 \)?
CMOS Inverter

Trip voltage moves with W/L

• Would you expect VIL, etc. to move with W/L?

How would you design an inverting receiver where input high noise and low noise have approx. equal magnitudes?
Shifting Trip Voltage $V_{th}$

Complete:

$V_{DD} = 5 \text{ V}$

$V_{T0,n} = 1.0 \text{ V}$

$V_{T0,p} = -1.0 \text{ V}$

$k_R = 0.25$

$k_R = 1.0$

$k_R = 4.0$

$k_R = \frac{k_n}{k_p}$

Figure 5.24 Voltage transfer characteristics of three CMOS inverters, with different nMOS-to-pMOS ratios.

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**Transient (Step) Response**

Idealized Input: Unit step

Equivalent Circuit:

- $V_o \geq V_{DD} - V_{tn}$
- $t = 0$
- $V_o < V_{DD} - V_{tn}$

90% - 10% Fall Time

$$C_L \frac{dV_o}{dt} + I_{DS} = 0$$

$$t_f = C_L \int_{V_{DD} - V_{tn}}^{0.9V_{DD}} I_{DS(satn)}dV_o + \int_{0.9V_{DD}}^{V_{DD} - V_{in}} I_{DS(linear)}dV_o$$

$$t_f \approx 4 \frac{C_L}{\beta_n V_{DD}}$$
**Constant Current Approximation**

Actual Input: Ramp
Step response vs. response to input with rise time = output fall time

\[ \tau = \frac{V_{DD}C_L}{I_{DSS}} \]

(IDSS = Satn current)

See Poulton and Dally for “derivation”
**Constant Current – Rise Time**

Input rise time affects output delay:

\[
V_{\text{inv}} \quad T_{\text{PHL}} \approx \tau t^{0.5} \\
2r \tau \quad 2r \tau
\]

\[
V_{\text{inv}} \quad T_{\text{PHL}} \approx \tau (1-r)
\]

See text for derivation.
Inverter as Small Signal Amplifier

Can be used to restore small swing “logic” (e.g. input from lossy channel)

- Gain in high-gain region
  \[ \text{Gain} = \frac{4}{(V_{GS}-V_T)(\lambda_p+\lambda_n)} \]
  About 20-40 practically
- Note: Miller effect increases apparent input capacitance in high gain region
- Frequency Response:
  - \[ \frac{dv_{out}}{dt} = \frac{i}{C} = g_m \frac{v_{in}}{C} = \frac{I_{DSS}}{V_{DD}} \frac{v_{in}}{C} \]
  - Sinusoid: \( v_{out} = \sin \omega t = A v_{in} \)
    \[ \frac{dv_{out}}{dt} = \omega \sin \omega t \]
    \[ \text{When } A=1 : \omega_1 = \frac{I_{DSS}}{V_{DD}} C = \frac{1}{\tau} \]
    \[ \text{i.e. } f_1 = \frac{1}{2\pi \tau} \]

\( f_1 \) called Gain-Bandwidth Product
**Miller Effect Capacitance**

Affects capacitance seen by small-signal equivalent circuit.

**Miller’s Theorem:**

Series capacitance in gain ckt:

\[
\text{Vin} \quad C_m \quad \text{Vout} = AVin
\]

Can be transformed to the following equivalent circuit:

\[
\text{Vin} \quad (1-A)C_m \quad \text{Vout} = AVin
\]

\( A \) is \(-ve\) ➔ Cin increases a lot in high gain region (at Vinv)

➔ Zin = \(1/j\omega Cin\) changes a lot in this region

Matters when constant known Zin matters
**Static Logic Gates**

Complementary pull-down and pull-up circuits

**Analysis & Design Issues**

- Body Effect changing Vtn for upper pull-up
- Transistor sizing:
  - Can speed up one path over another. (Note: Body effect on P2)
  - E.g. If path through ‘x’ is more critical, increase those transistors sizes.
  - If ‘y’ had to be faster (input arrived later in clock cycle) would it make sense to swap y with x?
Classic CMOS Gate

DC transfer characteristics

Reasoning:

\[ kn = 2kp \]

\[ \beta_{\text{pullup}} \propto kn; \quad \beta_{\text{pulldown}} \propto kn/2 \]
Transistor Sizing in Pull Down Logic

Want graded sizing for fastest transient operation:

\[
\text{Delay } \propto R3 (C1 + C2 + C3) + R2 (C1 + C2) + R1 C1
\]
Classic Static CMOS

NAND gate:

\[ f \propto \frac{kn}{2} \]

To equalize delays:

\[ p_1 \quad p_2 \]

\[ n_1 \quad n_2 \]

\[ x \quad y \]

\[ \beta_{\text{eff}} \propto \frac{kn}{2} \]

Higher CL (S of \( y \) nfet, D of \( x \)) reduced by body effect (\( f < 1 \))
Static CMOS Logic

Advantages:
- Low power
  - Only leakage when not switching
- High Noise Tolerance
- No clock needed
- Good target for automatic synthesis

Disadvantages:
- High fan-out load (lower speed)
  - pFET and nFET loads
- High noise generation (crowbar currents and I_{noise} = C_{load} \frac{dv}{dt})
- Delay scales poorly with logical width
  - E.g. Multi-bit OR & NOR (e.g. zero detect circuit) much slower in Static CMOS than in domino logic

= Slow
**Static CMOS Logic**

**Main Uses:**

- Automatic synthesis
- Random logic with low logic widths
- Logic or buffers with large loads
  - Ratio drivers
  - Not as much need to upsize pFETs to get equal rise and fall delays
  - Easier to drive large loads in Static CMOS than other styles
  - Can have logic in earlier stages

![Diagrams showing logic levels](image)
Reducing Power Consumption

1. Reduce Vdd
   - Energy per switching event $\propto Vdd^2$
   - Gate delay $\propto Idss = \beta(Vdd-VT)^2$
     - I.e. $\propto Vdd^2$
   - Power $\propto$ energy * fclock $\sim Vdd^4$
   - Tradeoffs Power with Delay:
     - Halve Vdd $\Rightarrow$ Quarter speed, one-Sixteenth the power
     - (until Vdd starts approaching 2 VT, at which delay goes up rapidly)
   - Only suited when speed penalty acceptable
   - Why not just drop VT?

[Graph: Energy-Delay Product as a Function of Supply Voltage]
Reducing Power Consumption

2. Variable Threshold Design
   2.A. By Adjusting Body Voltage
   \[ \text{VBp} = \text{Vdd (active)} \]
   \[ = 2 \times \text{Vdd (standby)} \]
   \[ \text{VBn} = \text{GND (active)} \]
   \[ = -\text{Vdd (standby)} \]

2.B. By using a multi-Vt process

High-Vt transistors at top and bottom block sub-threshold leakage path during standby operation
Biasing $V_{BS}$ shifts device $V_T$ higher (for reverse bias) or lower (for forward bias). Here, 4V reverse bias yields 800mV higher NMOS $V_T$.

Forward bias (FB) increases subthreshold current due to junction leakage.

Interesting note – PMOS reverse bias (RB) $V_T$ shift is limited for some reason, saturates at 300mV shift at 1.5V FB – impacts ability to use PMOS $V_{BS}$ to modify circuit properties.
New LOGIC transistor design with dynamic body contact enabled by pulling source/drain dopant across the gate poly extensions, creating two parasitic FETs between the drain and body contacts. Body $V_B$ determined by gate and drain voltage. All transistors are effectively “edgeless”, and the new transistor layout area is identical to the baseline transistor.
Low Power Digital

Minimize Energy·Delay product requires:

- Fast transitions (low Vt)
- Low leakage power (high Vt)

Electrical Results - Pass Gate Chain Delay vs. V$_{DD}$

25% savings in energy·delay

Damiano, Franzon
**DCVS Logic**

Differential Cascode Voltage Switch Logic

- pFETs form differential evaluate tree – half-latch pull-ups

\[
k_n = 2k_p
\]

Assume \( w = 1 \) initially

Assume \( A', B' \) fall symmetrically with \( A, B \)

\( f \) falls, turning \( p_1 \) on

\( t_f \propto 2k_n \)

\( t_r \propto k_n / 2 \)
**DCVS Logic**

**Advantages:**
- Low fanout load
  - Faster speed, and lower $I_{\text{noise}} = C \frac{dV}{dt}$
  - Good noise immunity (hysteris in latch, static)
  - No clocks
- Implicit inverse available (can save logic)
- Can have better logic density

**Disadvantages:**
- pFET fights pull-down chain
  - Higher crowbar current
- Higher device count in some applications

**Found to be particularly useful in ECC applications that benefit from rich XOR, XNOR trees**

High-speed on-chip ECC for synergistic fault-tolerance memory chips
Fifield, J.A.; Stapper, C.H.;
Solid-State Circuits, IEEE Journal of
DCVS logic

Transistor Size tradeoffs:

- In general:
  - Want $W_n \geq W_p$, so can overcome pFETs
- $(A,B) : (1,0) \rightarrow (1,1)$ or $(0,0) \rightarrow (1,1)$
  - Want $W_{n2} > W_{n1}$ so $n2$ can discharge $CL$ @ $f'$ quickly
- $(A,B) : (1,1) \rightarrow (1,0)$
  - $p1$ has higher $CL$ to charge (source of $n1$, drain of $n2$)
  - Try to turn $p1$ on quicker by turning $n4$ on quicker
  - $W_{n4} > W_{n3}$?
- Have to balance against $CL$ on previous stage
Transmission Gates

Pass Gates:

• What is the limitation of an n-type pass gate?

\[ X = VDD \]

• Fix with a transmission gate:

Use for:
• Logic, esp. muxes
• Bi-directional structures
  • E.g. Segmented buses
Pass Gate Logic

Multiplexor:

What does the following do?

When is the only time you would use it?

Only when a high impedance connection is desired. e.g. shared busses. Accidental high impedance connections can lead to floating nodes and logic errors.
Delay in Pass Logic

Regions of operation:

<table>
<thead>
<tr>
<th>Region</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>(</td>
<td>V_{GS}</td>
</tr>
<tr>
<td>(</td>
<td>V_{GS}-V_T</td>
</tr>
<tr>
<td>(V_{DS} \geq</td>
<td>V_{GS}-V_T</td>
</tr>
</tbody>
</table>

RC delay model appropriate
Complementary Pass Logic

Concept:

- Save area on Transmission Gate or other fully complementary style by using an nMOS pass gate instead of Transmission Gate
  - Restore using an inverter
  - Prefer low-Vt nMOS transistors
  - Compromises noise margin

\[ f = (A \cdot B)' \]

Note: \( f \) and \( f' \) are fully specified for all values of \( A, B \) (i.e., inverter input never floating.)
DCVS with Pass Gate

Advantages
- Speed, power
- Does not have pFET sensitivity of DCVS
  - PG logic pulls UP as well as down
- Reduced device count
- Good noise immunity

Disadvantages
- Body Effect
- Limited fan-in
- Limited load drive
**DPL**

**Double Pass Transistor Logic**

- Provides improved noise margin through incorporation of pFETs

![Diagram of XOR using high-performance DPL](image-url)
**Swing Restored Pass Gate Logic**

Add pull-downs
- Creates cross-coupled latch

Advantages:
- Improves noise tolerance
- Improves speed due to latch amplifier

Disadvantages
- Cross-over current
- Limited output drive (still)
Energy-Economized Pass Transistor Logic (EEPL)

Operation:
(B=1)

Initially
- \( I_1 \) high, \( I_2 \) low (\( p_1 \) off, \( p_2 \) on)
- \( A \rightarrow 0 \)
- \( A \) pulls \( I_1 \) low \( \rightarrow \) \( p_1 \) on; \( p_4 \) on; \( f' \rightarrow \) high
- \( A' \) pulls \( I_2 \) to \( Vdd-Vt \) \( \rightarrow \) \( p_2 \) OFF; \( n_6 \) on; \( f \rightarrow \) low
- \( I_2 \) eventually pulled to \( Vdd \) via \( p_1 \) after \( f' \) high

\( p_1, p_2 \) prevent cross-over current, reducing power consumption
Complementary Pass Gate Logic

Advantages:
- High speed
- Low power
- Esp. In low-Vt process

Disadvantages
- Body effect
- Limited fan-in
- Reduced noise margin

Main Uses:
- Usually faster Muxes, byte aligners, barrel shifters than other logic styles
- Low-power arithmetic circuits
... CPL

<table>
<thead>
<tr>
<th>Parameters (Vdd=3.3 V)</th>
<th>Static</th>
<th>CPL</th>
<th>DPL</th>
<th>Dual Rail Domino</th>
<th>Single Rail Domino</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power @ 100 MHz</td>
<td>34.3</td>
<td>34.5</td>
<td>27.5</td>
<td>82.5</td>
<td>60.2</td>
<td>mW</td>
</tr>
<tr>
<td>percentage</td>
<td>125</td>
<td>125</td>
<td>100</td>
<td>300</td>
<td>219</td>
<td>%</td>
</tr>
<tr>
<td>Delay of critical path</td>
<td>2.33</td>
<td>2.24</td>
<td>1.98</td>
<td>1.78</td>
<td>1.64</td>
<td>ns</td>
</tr>
<tr>
<td>Percentage</td>
<td>142</td>
<td>137</td>
<td>121</td>
<td>109</td>
<td>100</td>
<td>%</td>
</tr>
<tr>
<td>Energy @ 100 MHz</td>
<td>79.9</td>
<td>77.3</td>
<td>54.5</td>
<td>146.9</td>
<td>98.7</td>
<td>pJ</td>
</tr>
<tr>
<td>Percentage</td>
<td>147</td>
<td>142</td>
<td>100</td>
<td>270</td>
<td>181</td>
<td>%</td>
</tr>
<tr>
<td>Area: pMOSFET width</td>
<td>17700</td>
<td>8295.6</td>
<td>11935.5</td>
<td>14716.4</td>
<td>12064.4</td>
<td>μm</td>
</tr>
<tr>
<td>nMOSFET width</td>
<td>9655</td>
<td>9141.5</td>
<td>7181</td>
<td>17728</td>
<td>14862</td>
<td>μm</td>
</tr>
<tr>
<td>total tr. width</td>
<td>27355</td>
<td>17437.1</td>
<td>19116.5</td>
<td>32444.4</td>
<td>26926.4</td>
<td>μm</td>
</tr>
<tr>
<td>Percentage</td>
<td>157</td>
<td>100</td>
<td>110</td>
<td>186</td>
<td>154</td>
<td>%</td>
</tr>
</tbody>
</table>

Low-power design techniques for high-performance CMOS adders
Uming Ko; Balsara, T.; Wai Lee;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 3, Issue 2, June 1995 Page(s):327 - 333
Summary

What 2 performance figures does the saturated DS current, IDSS, of a transistor determine?

In a gate pull down chain, how might the transistors be sized?

\[ A \uparrow \quad n_1 \quad \downarrow \quad B \]

\[ B \uparrow \quad n_2 \quad \downarrow \]

How are multi-Vt processes used?
Summary

What is the main potential advantage of DCVS?

What is the main potential advantage of Pass Transistor Logic?