Static Combinational Circuits

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Outline

1. CMOS Inverter
   • DC and AC characteristics
2. Static logic gates
   • Structure
   • Relative transistor sizing
   • Multi-Vt circuits
3. Differential Cascode Voltage Switch (DCVS) Logic
   • Structure
   • Transistor Sizing
4. Pass Gate Logic
   • Structures & Alternatives
   • Transistor Sizing

References:
   Dally & Poulton, Chapters 4, 12.1
Basic CMOS Circuit Analysis

Core Principle:

Analysis of any digital circuit usually revolves around determining the transistor states for each region of operation.

Basic Approach:
1. Estimate states or voltages
2. Calculate voltages or states
3. Make sure self-consistent

<table>
<thead>
<tr>
<th>Region</th>
<th>State</th>
<th>Equivalent Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>V_{GS}</td>
<td>&lt;</td>
</tr>
<tr>
<td>$</td>
<td>V_{GS}-V_T</td>
<td>&gt; V_{DS} \geq 0$</td>
</tr>
<tr>
<td>$V_{DS} \geq</td>
<td>V_{GS}-V_T</td>
<td>\geq 0$</td>
</tr>
</tbody>
</table>

$G \rightarrow \text{Source of “majority carriers”}$

$e^{-}$ in nmos case, $p^{+}$ in pmos

CMOS Inverter

Static CMOS Inverter:

- Transfer Characteristic:

1: $V_{in} = 0$, $V_{out} = V_{dd}$
   - N: $V_{GS}$=0, $V_{DS}$= 3.3, $|V_{GS}| < |V_T|$ : Off
   - P: $V_{GS}$=3.3, $V_{DS}$=0, $V_{GS}-V_T| > V_{DS}$ : LINEAR

2: $V_{in} > |V_T|$ | $|V_{GS}| < |V_T|$ |
   - N: $V_{GS}$=1, $V_{DS}$=3, $V_{DS} \geq |V_{GS}-V_T|$ : SATN
   - P: $V_{GS}$=3, $V_{DS}$=0, $V_{GS}-V_T| > V_{DS}$ : LINEAR

3: $V_{in} \sim V_{out}$
   - N: $V_{GS}$=1.6, $V_{DS}$=1.6, $V_{DS} \geq |V_{GS}-V_T|$ : SATN
   - P: $V_{GS}$=1.6, $V_{DS}$=0.3, $V_{GS}-V_T| > V_{DS}$ : LINEAR

3: High Gain Region

Gain = $\frac{4}{(V_{GS}-V_T)(\lambda_p + \lambda_n)}$

To simplify, use $V_{dd}$=3.3 V

| VT | = 0.5 V in examples

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CMOS Inverter

“Trip” Voltage
- where Vout = 0.5 VDD
  - Both nFET and pFET in saturation
  \[ I_{DSn} = -I_{DSP} \]
  \[ \frac{\beta_n}{2} (V_{in} - V_{Tn})^2 = -\frac{\beta_p}{2} (V_{in} - V_{DD} - V_{Tp})^2 \]
  \[ V_{in} = \frac{V_{DD} + V_{ppp} + V_{in} \sqrt{\beta_n / \beta_p}}{1 + \sqrt{\beta_n / \beta_p}} \]
- If \( \beta_n = \beta_p \) and \( V_{tn} = -V_{tp} \), \( V_{in} = VDD/2 \)  
  \( (1.65 \text{ V with parameters on prev. page}) \)
- What if \( \beta_n = 2 \beta_p \), \( W_n/L_n = W_p/L_p \), \( VDD = 3.3 \), \( V_{tn} = -V_{tp} = 0.5 \)?

Trip Voltage changes with \( \beta \) and \( V_t \)
- Esp. W/L

CMOS Inverter

Trip voltage moves with W/L
- Would you expect VIL, etc. to move with W/L?

How would you design an inverting receiver where input high noise and low noise have approx. equal magnitudes?
**Shifting Trip Voltage Vth**

Complete:

$$k_R = \frac{k_n}{k_p}$$

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**Transient (Step) Response**

**Idealized Input:** Unit step

- **Linear Discharge:** $V_o \geq V_{DD} - V_{th}$
- **Exponential:** $V_o < V_{DD} - V_{th}$

**Equivalent Circuit:**

- **90% - 10% Fall Time**

$$\tau_f \approx 4 \frac{C_s}{\beta V_{DD}}$$
**Constant Current Approximation**

Actual Input: Ramp

Step response vs. response to input with rise time = output fall time

\[ \tau = \frac{V_{DD} C}{I_{DSS}} \]

(IDSS = Satn current)

See Poulton and Dally for “derivation”

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**Constant Current – Rise Time**

Input rise time affects output delay:

\[ TPHL \approx \tau \]

\[ TPHL \approx \tau^{0.5} \]

\[ TPHL \approx \tau(1-r) \]

See text for derivation.
**Inverter as Small Signal Amplifier**

Can be used to restore small swing “logic” (e.g. input from lossy channel)

- Gain in high-gain region
  \[ \text{Gain} = \frac{4}{(V_{GS} - V_T)(\lambda_p + \lambda_n)} \]
  About 20-40 practically

- Note: Miller effect increases apparent input capacitance in high gain region

- Frequency Response:
  \[ \frac{dv_{\text{out}}}{dt} = \frac{i}{C} = \frac{g_m v_{\text{in}}}{C} = \frac{I_{\text{DSS}}}{V_{DD}} \frac{v_{\text{in}}}{C} \]

- Sinusoid: \[ v_{\text{out}} = \sin \omega t = A v_{\text{in}} \]
  \[ \Rightarrow \frac{dv_{\text{out}}}{dt} = \omega \sin \omega t \]
  \[ \Rightarrow \text{When } A=1: \quad \omega = \frac{I_{\text{DSS}}}{V_{DD}C} = \frac{1}{\tau} \]
  \[ \Rightarrow f_1 = \frac{1}{2\pi \tau} \]

- \( f_1 \) called Gain-Bandwidth Product

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**Miller Effect Capacitance**

Affects capacitance seen by small-signal equivalent circuit.

Miller’s Theorem:

Series capacitance in gain ckt:

\[ \text{Can be transformed to the following equivalent circuit:} \]

\[ A \text{ is } -\text{ve} \Rightarrow \text{Cin increases a lot in high gain region (at Vinv)} \]

\[ \Rightarrow Z_{\text{in}} = \frac{1}{j\omega \text{Cin}} \text{ changes a lot in this region} \]

\[ \Rightarrow \text{Matters when constant known Zin matters} \]
Static Logic Gates

Complementary pull-down and pull-up circuits

Analysis & Design Issues
- Body Effect changing Vtn for upper pull-up
- Transistor sizing:
  - Can speed up one path over another. (Note: Body effect on P2)
  - E.g. If path through ‘x’ is more critical, increase those transistors sizes.
  - If ‘y’ had to be faster (input arrived later in clock cycle) would it make sense to swap y with x?

Classic CMOS Gate

DC transfer characteristics

Reasoning:
Transistor Sizing in Pull Down Logic

Want graded sizing for fastest transient operation:

\[
\text{Delay} \propto R_3 (C_1 + C_2 + C_3) + R_2 (C_1 + C_2) + R_1 C_1
\]

Classic Static CMOS

NAND gate:

\[ k_{n} = 2k_{p} \]

To equalize delays:

\[ n_1, n_2 \text{ (} n_2 > n_1 \text{)} \]

\[ p_1 \text{ (} p_2 > p_1 \text{)} \]

Possible Solution underlined
Static CMOS Logic

Advantages:

- Low power
  - Only leakage when not switching
- High Noise Tolerance
- No clock needed
- Good target for automatic synthesis

Disadvantages:

- High fan-out load (lower speed)
  - pFET and nFET loads
- High noise generation (crowbar currents and \( I_{\text{noise}} = C \frac{dv}{dt} \))
- Delay scales poorly with logical width
  - E.g. Multi-bit OR & NOR (e.g. zero detect circuit) much slower in Static CMOS than in domino logic

Main Uses:

- Automatic synthesis
- Random logic with low logic widths
- Logic or buffers with large loads
  - Ratio drivers
    - Not as much need to upsize pFETs to get equal rise and fall delays
    - Easier to drive large loads in Static CMOS than other styles
    - Can have logic in earlier stages
Reducing Power Consumption

1. Reduce Vdd
   - Energy per switching event $\propto Vdd^2$
   - Gate delay $\propto I_{dss} = \beta(Vdd-VT)^2$
     - i.e. $\propto Vdd^2$
   - Power $\propto$ energy * fclock $\sim Vdd^4$
   - Tradeoffs Power with Delay:
     - Halve Vdd $\Rightarrow$ Quarter speed, one-Sixteenth the power
     - (until Vdd starts approaching 2 VT, at which delay goes up rapidly)
     - Only suited when speed penalty acceptable
     - Why not just drop VT?

2. Variable Threshold Design
   2.A. By Adjusting Body Voltage
   2.B. By using a multi-Vt process

   High-Vt transistors at top and bottom block sub-threshold leakage path during standby operation
**IMPACT OF BODY BIAS**

Biasing $V_{BS}$ shifts device $V_T$ higher (for reverse bias) or lower (for forward bias). Here, 4V reverse bias yields 800mV higher NMOS $V_T$.

Forward bias (FB) increases subthreshold current due to junction leakage.

Interesting note – PMOS reverse bias (RB) $V_T$ shift is limited for some reason, saturates at 300mV shift at 1.5V FB – impacts ability to use PMOS $V_{BS}$ to modify circuit properties.

New LOGIC transistor design with dynamic body contact enabled by pulling source/drain dopant across the gate poly extensions, creating two parasitic FETs between the drain and body contacts. Body $V_B$ determined by gate and drain voltage. All transistors are effectively “edgeless”, and the new transistor layout area is identical to the baseline transistor.
**Low Power Digital**

Minimize Energy.Delay product requires:
- Fast transitions (low Vt)
- Low leakage power (high Vt)

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**DCVS Logic**

Differential Cascode Voltage Switch Logic
- pFETs form differential evaluate tree - half-latch pull-ups

- $f$ falls, turning $p_1$ on
- $t_f \propto 2k_n$
- $t_{r} \propto k_n/2$

\[ kn = 2kp \]

Assume $w=1$ initially
Assume $A'$ $B'$ fall symmetrically with $A$, $B$
DCVS Logic

Advantages:
- Low fanout load
  - Faster speed, and lower Inoise=Cdv/dt
  - Good noise immunity (hysteris in latch, static)
  - No clocks
- Implicit inverse available (can save logic)
- Can have better logic density

Disadvantages:
- pFET fights pull-down chain
  - Higher crowbar current
- Higher device count in some applications

Found to be particularly useful in ECC applications that benefit from rich XOR, XNOR trees

Transistor Size tradeoffs:
- In general:
  - Want Wn ≥ Wp, so can overcome pFETs
  - (A,B) : (1,0) → (1,1) or (0,0) → (1,1)
    - Want Wn2 > Wn1 so n2 can discharge CL @ f quickly
  - (A,B) : (1,1) → (1,0)
    - p1 has higher CL to charge (source of n1, drain of n2)
    - Try to turn p1 on quicker by turning n4 on quicker
    - Wn4 > Wn3?
- Have to balance against CL on previous stage

High-speed on-chip ECC for synergistic fault-tolerance memory chips
Fife, J.A.; Slappey, C.H.;
Solid-State Circuits, IEEE Journal of
**Transmission Gates**

Pass Gates:
- What is the limitation of an n-type pass gate?

\[ X = V_{DD} \]

- Fix with a transmission gate:

Use for:
- Logic, esp. muxes
- Bi-directional structures
  - E.g. Segmented buses

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**Pass Gate Logic**

Multiplexor:

What does the following do?

When is the only time you would use it?
**Delay in Pass Logic**

Regions of operation:

- **Vin=Vdd Out=0**
- **Vin=Vdd-Out=Vdd-Vtn**
- **Vin=Vtp-Out=Vdd**

<table>
<thead>
<tr>
<th>Region</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>(</td>
<td>V_{GS}</td>
</tr>
<tr>
<td>(</td>
<td>V_{GS}-V_T</td>
</tr>
<tr>
<td>(V_{DS} \leq</td>
<td>V_{GS}-V_T</td>
</tr>
</tbody>
</table>

**RC delay model appropriate**

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**Complementary Pass Logic**

Concept:
- Save area on Transmission Gate or other fully complementary style by using an nMOS pass gate instead of Transmission Gate
  - Restore using an inverter
  - Prefer low-Vt nMOS transistors
  - Compromises noise margin

\[
\begin{align*}
f & = (A \cdot B)'
\end{align*}
\]
**DCVS with Pass Gate**

**Advantages**
- Speed, power
- Does not have pFET sensitivity of DCVS
  - PG logic pulls UP as well as down
- Reduced device count
- Good noise immunity

**Disadvantages**
- Body Effect
- Limited fan-in
- Limited load drive

**DPL**

**Double Pass Transistor Logic**
- Provides improved noise margin through incorporation of pFETs
Swing Restored Pass Gate Logic

Add pull-downs
- Creates cross-coupled latch

Advantages:
- Improves noise tolerance
- Improves speed due to latch amplifier

Disadvantages
- Cross-over current
- Limited output drive (still)

Energy-Economized Pass Transistor Logic (EEPL)

Operation: \((B=1)\)

Initially
- \(\Pi\) high, \(I_2\) low (\(p_1\) off, \(p_2\) on)
- \(A \rightarrow 0\)
- \(A'\) pulls \(I_2\) to \(V_{dd}-V_t\) \(\rightarrow p_2\) OFF; \(n_6\) on; \(f \rightarrow low\)
- \(I_2\) eventually pulled to \(V_{dd}\) via \(p_1\) after \(f'\) high

\(p_1, p_2\) prevent cross-over current, reducing power consumption
Complementary Pass Gate Logic

Advantages:
- High speed
- Low power
- Esp. in low-Vt process

Disadvantages
- Body effect
- Limited fan-in
- Reduced noise margin

Main Uses:
- Usually faster Muxes, byte aligners, barrel shifters than other logic styles
- Low-power arithmetic circuits

\[ f = \overline{(A \cdot B)} \]

\[ S0 \quad S1 \]
\[ D0 \quad D1 \]

CPL Mux

TABLE III

<table>
<thead>
<tr>
<th>Parameters (VDD=3.3 V)</th>
<th>Static</th>
<th>CPL</th>
<th>DPL</th>
<th>Dual Rail</th>
<th>Single Rail</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power @ 100 MHz</td>
<td>34.3</td>
<td>34.3</td>
<td>27.5</td>
<td>42.5</td>
<td>60.2</td>
<td>mW</td>
</tr>
<tr>
<td>Percentage</td>
<td>125</td>
<td>127</td>
<td>100</td>
<td>300</td>
<td>2.19</td>
<td>%</td>
</tr>
<tr>
<td>Delay of critical path</td>
<td>2.33</td>
<td>2.24</td>
<td>1.98</td>
<td>1.78</td>
<td>1.64</td>
<td>ns</td>
</tr>
<tr>
<td>Percentage</td>
<td>142</td>
<td>147</td>
<td>131</td>
<td>100</td>
<td>100</td>
<td>%</td>
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<tr>
<td>Energy @ 100 MHz</td>
<td>19.9</td>
<td>17.3</td>
<td>14.5</td>
<td>146.9</td>
<td>91.7</td>
<td>pJ</td>
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<tr>
<td>Percentage</td>
<td>147</td>
<td>142</td>
<td>100</td>
<td>270</td>
<td>181</td>
<td>%</td>
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<tr>
<td>Active MOSFET width</td>
<td>17700</td>
<td>8235.6</td>
<td>11055.5</td>
<td>14516.4</td>
<td>12056.4</td>
<td>( \mu m )</td>
</tr>
<tr>
<td>nMOSFET width</td>
<td>9655</td>
<td>9141.5</td>
<td>7181</td>
<td>17728</td>
<td>14462</td>
<td>( \mu m )</td>
</tr>
<tr>
<td>total w. width</td>
<td>22235</td>
<td>17437.1</td>
<td>19316.5</td>
<td>32444.4</td>
<td>26926.4</td>
<td>( \mu m )</td>
</tr>
<tr>
<td>Percentage</td>
<td>157</td>
<td>100</td>
<td>110</td>
<td>186</td>
<td>154</td>
<td>%</td>
</tr>
</tbody>
</table>

Low-power design techniques for high-performance CMOS adders
Uming Ko; Bansara, T. Wai Lee.
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 3, Issue 2, June 1995 Page(s):327 - 333
Summary

What 2 performance figures does the saturated DS current, IDSS, of a transistor determine?

In a gate pull down chain, how might the transistors be sized?

\[
\begin{array}{c}
A \\
\downarrow \\
\text{smaller}
\end{array}
\quad
\begin{array}{c}
B \\
\downarrow \\
\text{larger}
\end{array}
\]

How are multi-Vt processes used?

Reduced Fanout load
Reduced Capacitance/switched node
Lower power

What is the main potential advantage of DCVS?

What is the main potential advantage of Pass Transistor Logic?