Signaling

Dr. Paul D. Franzon

Global Outline

• Interconnect Structures and Models
• Signaling
• Driver & Receiver circuits

References

• Dally & Poulton, Chapters 3, 5, 6, 7, 8
Outline

Basic Transmission Alternatives
- Synchronization Alternatives
- Single-side vs. Differential
- Directional vs. Bi-directional

Goals in High Speed Signaling
- Overview
- Bit Error Rate
- Jitter

Use of Signal Processing in High-Speed Channels
- Need for signal processing
- Time and Frequency domain alternatives
- Alternative implementations

Data Coding
Run time and spatial codes
Future Trends
Timing Scenarios

• Sufficient delay slack for noise to settle:

- If $t_{\text{interconnect-max}} < 5 \times \text{line delay}$, then design is very simple.

• First Incident Switching:

- If $t_{\text{interconnect-max}} < 5 \times \text{line delay}$, then design is very simple.
…Timing Scenarios

Source-Synchronous Switching

- Send clock with data
  - (or recover clock from data)

In such systems, the rise-times and skew from inter-symbol noise, processing and temperature variations determines maximum signal speeds

E.g. 2 Gbps, 30 inch wire

\[ t_{\text{symbol}} = 500 \text{ ps} \]
\[ t_{\text{wire}} = 5 \text{ ns} \]

If clock jitter has to be less than 10% of \( t_{\text{symbol}} \), \( t_{\text{jitter}} = 50 \text{ ps} \)

What % variation in clock “\( t_{\text{wire}} \)” would be acceptable? 1%

If a via \( C_L = 1 \text{ pF} \), \( Z_0 = 50 \text{ Ohm} \), what is the \( \tau \) of a via? 50 ps

Meeting such timing constraints over long distances is very hard.
Timing Scenarios

Clock & Data Recovery

- Recover clock from the data so that delay does not need to be precisely controlled.

- **Issues:**
  - Ensuring enough edges in data signal to generate clock
  - Design of clock recovery circuit (Phase Locked Loop, Delay Locked Loop)
Single sided vs. Differential

Cost:
- Full differential doubles board real-estate, and pin-count

Performance

- **Sensitivity:** Smallest RX input to give full swing at output (limited by gain A)
  - >~300 mV
  - ~100 mV
  - ~ +/- 50 mV (100 mV swing)
    +/− 20 mV with offset cancellation

- **Noise:**
  - **TX:** TX transmits substantial portion of power/gnd noise as CM noise
  - **RX:** Amplifies noise at input as normal

- **Noise on Tran line behaves as differential noise**
  - Rejects CM noise on input signal

- TX has low CM gain
  ⇒ Most power/gnd noise rejected
BiDirectional Signalling

Halves number of wires and pins!

Current Mode Version:

- Estimates $V_{\text{transmit}}$ from TX and subtracts it from signal at pin
- Speed limited compared with single sided as estimate is imperfect (due to package, $R_{\text{term}}$ mismatch, etc.) and ISI tends to be larger
- Voltage mode and differential versions

Hard to get working at high data rates

- Common to use DM in one direction and slow CM signaling in reverse direction
High Speed Design Goals

Main Goals

• Data Rate

• Bit Error Rate (BER)
  • $10^{-12}$ for older systems
    • 1 error every 5 minutes @ 3 Gbps
  • $10^{-15}$ today; $10^{-18}$ to $10^{-21}$ tomorrow
  • Limited by ability to resolve “0” or “1” in presence of noise and jitter

• Power Consumption
  • Today 10 – 30 mW @ 3 Gbps (including clock and data recovery (CDR))
  • Tomorrow: 2 mW per Gbps

Secondary Goals

• Minimize driver area
  • Make easy to place and route
**Bit Error Rate**

Best determined through experimentation
- Apply pseudo-random test pattern
- Measure logical output for bit value errors
- Requires full $2^{N-1}$ patterns to be effective
  - One worst case pattern is possible

Can be evaluated via eye diagram
- Only suitable technique at lower BERs
- E.g. At 3 Gbps, establishing a BER of less than $10^{-12}$ requires 6 minutes of error-free operation, while establishing a BER of less than $10^{-18}$, requires 10 years
- Provides an estimate only
  - Often leaves out specific noise sources
  - Relies on Gaussian Distribution
**Eye Diagram**

Send random data sequence down the channel
Measure output waveform
Superimpose all bit intervals on one Unit Interval (UI)

Clock

Data

Intersymbol Interference

Open Eye

One clock period or Unit Interval (UI)
Eye Diagram Analysis

Procedure:
- Captures InterSymbol Interference (ISI)
  - “leftover” noise from previous bits
- RMS Jitter = $\sigma_t$
  - Jitter in both signal and clock in practice!
  - (signal jitter included in -max values)
- Bit Error Rate (BER)
  - Related to Q Factor
  - $Q$ factor = $((P_1-P_0)/(\sigma_1-\sigma_0))$
  - For evaluation only – not true BER!

Sample:

$$BER = \frac{1}{2} \text{erfc}\left(\frac{Q}{\sqrt{2}}\right) \approx \frac{\exp(-Q^2/2)}{Q\sqrt{2\pi}}$$

<table>
<thead>
<tr>
<th>Q</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>$-10^{-9}$</td>
</tr>
<tr>
<td>7</td>
<td>$-10^{-12}$</td>
</tr>
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</table>

$Q$-factor tends only to be used for optical channels but demonstrates statistical basis for BER estimation.
Estimate BER from Eye Diagram

Note: Here we assume the signal is gauss distributed.

BER is expressed here by the shadow area:

Blue shadow for BER of ‘1’
Red shadow for BER of ‘0’

BER = Integration of the shadow area

RX sensitivity + offset due to variations
**Time Domain Errors**

Signal Jitter captured in eye diagram

- **Tbit (UI)**
- Clock Jitter

\[ P(\text{error}) = \text{area under these curves} \]
BER = \int_{NMH}^{\infty} \frac{1}{\sigma_1 \sqrt{2\pi}} \cdot \exp\left(-\frac{x^2}{2\sigma_1^2}\right) dx + \int_{NML}^{\infty} \frac{1}{\sigma_0 \sqrt{2\pi}} \cdot \exp\left(-\frac{x^2}{2\sigma_0^2}\right) dx

= \frac{1}{2} \text{erfc}\left(\frac{NMH}{\sqrt{2\sigma_1}}\right) + \frac{1}{2} \text{erfc}\left(\frac{NML}{\sqrt{2\sigma_0}}\right)

if \ \sigma_0 = \sigma_1 = \sigma, NMH = NML = 0.6V,

BER = \text{erfc}\left(\frac{NM}{\sqrt{2\sigma}}\right) \leq 10^{-12} \quad \iff \quad \sigma = \frac{NM}{7} \leq 0.085V

BER = \text{erfc}\left(\frac{NM}{\sqrt{2\sigma}}\right) \leq 10^{-17} \quad \iff \quad \sigma = \frac{NM}{8.6} \leq 0.07V

How to find \(\sigma\)?

Note: Here we assume the signal is gauss distributed.
Bathtub curve

Plot of BER vs. Eye closure

Figure 23. Timing bathtub curve

Figure 24. Voltage bathtub curve

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Accurate Method for Analyzing High-Speed I/O System Performance

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Chris Madden, Rambus Inc.
Vladimir Stojanovic, Massachusetts Institute of Technology
**BER Profile**

Can plot BER as contours against potential sampling constraints:

**Fig. 18.** Eye Diagram  
**Fig. 21.** BER contours before consider clock jitter  
**Fig. 22.** BER contours after sampling with clock
Another Example

Showing phase noise due to clock and data recovery (CDR)

Figure 2.1 A: Statistical eye diagram with CDR hold; B: CDR steady state phase distribution; C: BER contour conditioned with CDR distribution [5].
SNR View

BER determined by Signal to Noise ratio at RX output

\[ SNR = \frac{d_{\text{min}}^2}{\sigma^2} \]

\[ \text{Pr}_{\text{err}} = \frac{1}{2} \text{erfc} \left( \frac{\sqrt{SNR}}{2\sqrt{2}} \right) \]

where

- \( d_{\text{min}} \) = smallest separation of received data values @ RX (i.e. Signal power is \( d_{\text{min}}^2 \))
- \( \sigma^2 \) is the variance of noise at RX

Then, approximately
- BER of \( 10^{-12} \) requires a SNR of 23 dB
- BER of \( 10^{-15} \) requires a SNR of 24 dB

Sources of Eye Closure

Voltage Domain:
- Inter Symbol Interference (ISI) due to reflection noise
- ISI due to frequency-dependant loss in channel
- Crosstalk noise (when modeled)
- Simultaneous Switching Noise (SSN) (when modeled)
  - Self-induced
  - Induced to other circuits (other I/O, on-chip ckts)

Time Domain
- Signal jitter
- Clock jitter (phase noise)
- Jitter divided into
  - Deterministic Jitter (DJ)
  - Random Jitter (RJ)
- Total Jitter $TJ(BER) = DJ + \alpha(BER).RJ$
  - $\alpha$ is a confidence interval on the Gaussian above

<table>
<thead>
<tr>
<th>Table I. Various noise components of typical serial interface</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dynamic</strong></td>
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<tr>
<td>-------------</td>
</tr>
<tr>
<td>Random</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Deterministic</td>
</tr>
<tr>
<td>Static</td>
</tr>
</tbody>
</table>
ISI Due to Reflection Noise

Can obtain from Channel Impulse Response:
Measurement technique (TDR & TDT):

![Diagram](image)

- Fast Edge
- Reflected response
- Step Response
- SMA Card Connector Backplane

![Differentiate Step Response](image)

- Impulse response here

- [1], [2], etc.: Reflection Events

- [1-2]: 0.4 ns
- [1-2-1-5]: 0.8 ns
- [3-4]: 4.2 ns
- [3-5]: 4.4 ns

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Pulse Response or Single Bit Response

i.e. Time-domain result with a 010 input

Pre-cursor ISI (affects previous bits)

"cursor" location (this bit)

Post-cursor ISI (affects following bits)

UI
Pulse Response Shows Both Types of ISI

ISI due to “dispersion”
- Pulse spreads due to frequency-dependent losses
- Affects bits around cursor

ISI due to reflection and crosstalk noise
- Affects bits many UI after cursor

Raw Single Bit Response

Normalized single pulse @ TX

RX waveform after channel

c/- Zerbe, Rambus
**ISI Leads to Bit Failures**

- Middle sample is corrupted by 0.2 trailing ISI (from the previous symbol), and 0.1 leading ISI (from the next symbol) resulting in 0.3 total ISI
- As a result middle symbol is detected in error

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ISI due to Channel

Construct from Step Response

Pulse Response for Various Data Rates

Pulse response = +step followed by -step

Eyes for 101010
Eye Diagram

ISI Accumulation:

- ISI Accumulation from Step Response

   - Data Signal with ISI
   - Margin / Eye Opening
   - 141-mV Margin

   Eye for random data with maximum run length of 7.
Frequency-dependent attenuation in Channel produces inter-symbol interference (ISI):

Lone 1 in stream of 0’s undetectable

Equalization required when attenuation more than a few dB per octave
Effect of Channel Equalization

3-Ways to Look at Equalization

- Sharpen the Step Response
- Remove the Tail of the Pulse Response
- Flatten the Frequency Response to Nyquist

Tutorial ISSCC 2003
**Bit Error Rate Estimation**

**ISI Accumulation from Pulse Response**

- **0.36**
- **0.22**

- **No De-Emphasis**
- **60% De-Emphasis**
- **Equalized ISI**
- **Post-Cursor ISI**

- **Accumulated ISI**
- **RHS curve:** $\sum$ of post cursor points up to that point

- **Pulse tail at time bit count @ interval**

**Tutorial ISSCC 2003**
Signal Processing in Channels

Simplified System Model

- **TX Pre-Emphasis (Most common)**
  - Digital Finite Impulse Response (FIR) Filter
    - Most Common
    - Shapes pulse response (see above)
    - Reduces post-cursor ISI
    - Really “de-emphasis” – reduces signal swing

- **Linear Equalizer (less commonly present)**
  - Analog equalizer to remove pre-cursor ISI

- **Decision Feedback Equalizer (Becoming Common)**
  - Digital or analog to remove post-cursor ISI
Frequency Domain View

TX

Channel

Equalizing Filter

RX

Receiver Equalizer

Sampler

Clock

Equalized Channel

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**Time Domain View- Before & After Transmit Equalization**

Near-term ISI significantly improved

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Example: 5Gbps Over 26" of FR4 NoEq
Example: 5Gbps Over 26” of FR4 Under Equalized
Example: 5Gbps Over 26” FR4
Over Equalized

Note: Reduced swing
Example: 5Gbps Over 26” FR4
Correct Tx Equalization

Maximum SNR at the sample point
**TX pre-emphasis**

**Typical Structure:**
- FFE = Feed Forward Equalizer
- Filter Output
  \[ D_{out} = c_0 - c_1 z^{-1} - c_2 z^{-2} - c_3 z^{-3} \]

**Non-adaptive**
- Fixed Filter Weights
- For simple technique to calculate filter tap weights see project
- Note: Number of bits of post-cursor equalization = # delay cells in FF

**Adaptive**
- Learning sequence is used to calculate weights
- Requires “backchannel” – method for RX to send data to TX
Adaptive Architecture

Training sequence is used to determine tap weights

- Weights transmitted back to TX
  - E.g. Using slow Common Mode signal

![Diagram showing the adaptive architecture with FIR, C0, C1, C2, C3, D_IN, 1-bit delay blocks, summing node, and LMS optimizer.](image)
Three Basic Methods for Setting Equalization Coefficients

Lookup table ‘set and forget’
- Simple, based on lab measurement
- Subject to manufacturing and environment variations

Adapt once on power-up
- More complex
- Subject to environment variation

Continuous adaptation
- Most complex
- Most complete

What is really needed?
Simulation: 3.2G NRZ Set & Forget vs. Adapt Once
S&F optimized @ Zo, Both Sims @ hhh Corner

Variation is board-processing Zo
Simulation: 6.4G NRZ Set & Forget vs. Adapt Once
S&F optimized @ Zo, Both Sims @ hhh Corner

(a) Set & forget

(b) Adapt once

(c)
Measured prDFE/Tx4 Cycling 10C-85C
Receive Equalizer Filter

Decision Feedback Equalizer

Digital:
- Removes post-cursor ISI up to # of taps

Analog:
- First order shown (typically = to about 2 taps)

Linear Equalizer might add to correct for pre-cursor ISI and to correct for post-cursor ISI beyond # taps in filters
- Analog circuit
**Run Length Coding**

- Run length constrained and DC balanced codes

**Reasons to constrain max # and ratio of 1’s or 0’s**

- AC Coupled Signals
  - ![AC Coupled Signals Diagram](image)
  - **Want**: Fixed $V_{bias}$
  - ➔ Average value of input signal must be known
  - ➔ Known ratio of 0’s to 1’s
  - ➔ AC balanced signals

- (e.g. Fiber Channel)
- Provide sufficient edges for clock recovery
  - ➔ Max # of 1’s or 0’s in sequence known
- Reduce SSN, return current and $d/dt$(return current)
  - ➔ Balance 01 and 10 simultaneous transitions in a bus
**Concepts in Balanced Codes**

**Run Length**
- Max # of 1’s in sequence = rmax
- Min # of 1’s in sequence = rmin
- Code referred to as (rmin-1, rmax-1) code

**Bit Stuffing**
- Simplest way to achieve a (0,m) code is to insert a false bit when rmax hit
- Requires synchronization at frame level and counters at RX and TX
- E.g. Achieving (0,2)
  - Data : 0100001110
  - Encoded data: 010001011100
- Though reduces low frequency content, does not eliminate a DC bias drift
- Can not predict actual symbol rate
  - Can predict worst case symbol rate
    - What is it for (0,2)?
Disparity

- $= \# \text{ of 1's} - \# \text{ of 0's}$

Digital-Sum Variation (DSV)

- $= \text{Max. variation in disparity}$
- Constant DSV $\Rightarrow$ DC-balanced signal, $r_{\text{max}} = \text{DSV}$
- Determines low frequency components of signal

e.g. 8B10B code

- 8-bit Data Bytes encoded as 10-bit characters
- 12 control characters are encoded too
- Run length of 5
- DSV = 3
Block Codes

Nonoverlapping Block Codes

- Each block of \( n \) bits is coded as \( m \) bits with equal numbers of 1s and 0s
- Number of zero-disparity code words in \( m \) bits is \( \binom{m}{n/2} \)
- Number of input signals is \( 2^n \)
- Thus code exists if \( \binom{m}{n/2} > 2^n \)
- Code efficiency = \( n/m \)

E.g. \( n=2, m=4 \)

<table>
<thead>
<tr>
<th>input</th>
<th>code</th>
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<tr>
<td>00</td>
<td>0101</td>
</tr>
<tr>
<td>01</td>
<td>1010</td>
</tr>
<tr>
<td>11</td>
<td>1100</td>
</tr>
<tr>
<td>10</td>
<td>0011</td>
</tr>
</tbody>
</table>

Efficiency = 50%

- E.g. \( n = 8, m=12 \), efficiency = 67%
Running Disparity Codes

- Permits non-zero disparity in “code word”
- Constrains worst case disparity

- Disparity = disparity of current block
- Accum = accumulated disparity, including comp bit
- Compare = 1 if Disparity and Accum have same signs
  \[ = \sim(\text{sign}(\text{accum})) \text{ if disparity} = 0 \]
- Max run length = 2(n+1); Disparity ranges over \([-3n/2, 3n/2]\)
- DSV = 3n
- 8-bit burst error occurs whenever comp bit wrong
Spatial N of M Signalling

Used to reduce Common Mode noise in power/ground/return system

- Reduces SSN at TX
- Reduces signal return current
- e.g. Hamming Codes
Single Symbol Encoding

NRZ = Non Return to Zero
RZ = Return to Zero
Ternary ➔ 3 level signaling
PAM-4 ➔ Encode bit pair (symbol) as one of 4 levels

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
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<td>PAM-4</td>
<td></td>
<td></td>
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</table>
Other Encodings

RF-like:
- DQPSK (Differential Quadrature Phase Shift Keying)
- Multi-tone

Duobinary
- For strict definition see table on right
- Definition used in data comms:
  \[ \text{Out}_k = a_k + a_{k-1} \]
- Reduces frequency demands
- Allows some error detection & correction

<table>
<thead>
<tr>
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<th>NRZ</th>
<th>Duobinary</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>+1 if # 0’s since last 1 was even</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>-1 if # 0’s since last 1 was odd</td>
<td></td>
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PR-4 (partial response)
- Reduces frequency content
- E.g. PR-4:
  \[ \text{Out}_k = a_k - a_{k-2} \]
Symbol Encoding Tradeoffs

- **NRZ (also called PAM-2)**
  - Most common

- **RZ**
  - Requires 2* channel bandwidth of NRZ
  - (Only used in optical signals where BW is almost infinite)

- **Ternary NRZ**
  - Use against Vref in single-sided TX, differential RX

- **Ternary RZ**
  - DC balanced
  - Use against Vref in single-sided TX, differential RX

- **PAM-4**
  - Requires half channel BW of PAM-2
  - Reduced signal swing per symbol
  - Requires ADC at RX
  - Not useful unless channel BW very limited
Multi-level Signaling

2-PAM (NRZ) signaling simple & robust
- Operates at lowest BER for given SNR
But, may be difficult or impossible to equalize a “bad” channel sufficiently,
Or, severe crosstalk may use up margin
4-PAM signaling for “bad” channels
- 2 bits/baud
- Same bit rate at half the baud rate of 2-PAM
- But complicated receiver

Duobinary and PR-4
- Reduces bandwidth without complexity of PAM-4
- Requires slicer at RX with two decision levels
When should you use 4-PAM?

- If attenuation increases by more than 10dB over an octave, 4-PAM should be considered

2-PAM @ 6.25 Gbit/sec
4-PAM @ 3.125 Gbaud/sec
4-PAM Cautions

Eye height 1/3 of 2-PAM, so 10dB less amplitude per bit
Re-introduces the “reference problem” at the receiver (no reference needed for 2-PAM).
Edge trajectories close eye horizontally
2-PAM / 4-PAM crossover more like 15dB/octave
Comparisons

Fig. 2 Sample eye diagrams of NRZ, PAM4, DB and PR4 signaling [5].

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Comparison of Signaling and Equalization Schemes in High Speed SerDes (10-25Gbps)

(a)

(b)

Fig. 8. Frequency response (a) and pulse response (b) of an example channel.
Comparisons

Fig. 22. Performance comparison of NRZ, DB, and PAM4 signaling over the backplane shown in Fig 19 at data rate of 25Gb/s with the crosstalk shown in Fig. 20.

Although equalization and crosstalk cancellation are powerful tools, residual misalignment, reflections, as well as crosstalk are likely to reduce overall system performance.
Summary

What are the main factor(s) that cause eye closure?

How is equalization useful?

What are the advantages of single-sided TX, differential RX over single-sided RX?
... Summary

What is the advantage of a full differential system?

What are the uses of DC-balanced and run-length codes?

What is the potential advantage of PAM-4, Duobinary and PR-4 over PAM-2?