I/O Circuits

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Global Outline

• Interconnect Structures and Models
• Signaling
• Driver & Receiver circuits

References

• Dally & Poulton, Chapters 3, 5, 6, 7, 8
• F. Yuan, “CMOS Current-Mode Circuits for Data Communications”, Springer
• W.F. Egan, “Phase Lock Basics”, Wiley
Outline

• Current Mode Circuits
• SerDes Design
  • Driver and TX Eq
  • Receiver and RX Eq
  • PLL-based CDR
• Voltage Mode Circuits
• Receiver Timing Requirements
• ESD Protection
• On-chip termination
Current Mode Logic

Large Swing TX circuits
- Introduction
- Current Mirrors
- Design Approach

Small input swing amplifiers
- Introduction
- Design Approach
- Loads

Current Mode Latches
Large Swing Differential Ckts

Advantages:
- Speed
- True differential
- Low di/dt → low SSN

Can also be used for high speed differential logic (AND, OR, XOR):

```
OUT_N -- A
  |   |   |
  Vbias |   |
      A

OUT_P -- B
  |   |   |
  Vbias |   |
      B

OUT_P -- Ab
  |   |   |
  Vbias |   |
      Ab

OUT_N -- Bb
  |   |   |
  Vbias |   |
      Bb

IN_P -- M1
     |   |
     Vp |
     IN_N -- M2

Load

Differential Pair

Current Source
```

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Current Mirror

First order treatment

- **M1:**
  - $V_{DS}=V_{GS} \Rightarrow$ Satn
  - $I_{ref}=I_{DS}=k/2 \ W/L \ (V_{GS}-V_{T})^2$

- **M2, M3:**
  - As long as $V_{DS}$ large enough to put into saturation
  - $V_{GS2}=V_{GS3}=V_{GS1}$
  - $\Rightarrow$ If $L_1=L_2=L_3$, then

\[
\frac{I_2}{I_{ref}} = \frac{W_2}{W_1}, \quad \frac{I_3}{I_{ref}} = \frac{W_3}{W_1}
\]

- With Channel length modulation taken into account,

\[
\frac{I_2}{I_{ref}} = \frac{W_2/L_2}{W_1/L_1} \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}
\]

Long $L_1, L_2$ improves matching
Current Mirrors

(a) m1 diode connected & in saturation. When m2 in saturation

\[ I_2 = \beta (V_{GG} - V_{tn})^2 (1 + \lambda V_o) = I_1 (1 + \lambda V_o) \]

\[ r_o = \frac{\partial V_o}{\partial I_2} = \frac{1}{\lambda I_1} \]

- Make transistors long to reduce \( \lambda \)
- Add low pass filter to reduce CM noise from power/ground
- Note: Min voltage drop required over \( V_o \) to keep m2 in saturation
Large Swing Differential Drivers

Driver: Design for Large Swing at output

DC (Swing) Analysis:

M0 must remain in Saturation

\[ V_p > V_{tn} \text{ (0.1} \rightarrow 0.25 \text{ V depending on Vdd)} \]

ID1+ID2=I_{tail}

Swing limits at output:

- Determine by when M1 or M2 are off

\[
\begin{align*}
V_{\text{high}} &= V_{DD} \\
V_{\text{low}} &= V_{DD} - I_{tail} R
\end{align*}
\]

- Note: M1, M2 must be large enough to support I_{tail}

- Tradeoffs:
  - Increased swing requires high I_{tail} \rightarrow Increased power consumption
  - I_{tail} limited by requirement: V_{low} > V_p (see above)
Swing, Bandwidth and Power trade-off

**OUTPUT impedance**

- \( z = R \) at output High
- \( z = R \| R_{M1} \) at output Low
- Requires High \( R_{M1} \) to balance output impedance, put M1 and M2 into saturation will be best

**Lumped model** \( \tau = R \times C \) at output, \( C \) is the load

- High bandwidth means smaller \( R \)
  - That’s smaller output swing
  - Max swing is \( V_x = V_{dd} - I_{tail} \times R \)
- Increase \( I_{tail} \) can improve both bandwidth and Swing
  - But burns more power
Design Example:

Design specs:

- Input swing range: 1.16 to 1.8V
- Output swing range: same as above
- One transistor goes off at max swing
- Data rate $S=5\text{GHz}$ and Load $C_L=100\text{fF}$
- $V_{\text{thn}}=0.45\text{V} \sim 0.52\text{V}$, use 0.5V here
- Overdrive voltage margin=0.25V
- Length ($L$) of $M_0$, 2 to 3 times of $L_{\text{min}}$ to reduce short channel effect
### Design Procedure

#### Edge Rate

- $t_R \approx 2.2 \, RC$
- Want $t_R < t_{bit}$
  - $R < 1/(2.2 \cdot sC) = 900 \, \text{Ohm}$
  - e.g. Chose $R = 800 \, \text{Ohm}$

**Tail current**: $I_{tail} = (1.8-1.16)/R = 0.8 \, \text{mA}$

#### $V_p$:

- Keep $M_0$ in saturation and make sure $M_1$ and $M_2$ can turn off
- To keep $M_0$ in saturation implies $V_p > V_t$. E.g. $V_p = 0.75 \, \text{V}$ gives $0.25 \, \text{V}$ of margin
- To turn $M_1$ off, requires $V_p > V_{\text{In-low}} - V_t = 1.16 - 0.5 = 0.66 \, \text{V}$
- $V_p \geq 0.75 \, \text{V}$
... Design Procedure

M0 Sizing
- W/L to give \( I_{tail} \) at \( V_{bias} \)
- Make long to reduce impact of short channel effects

M1, M2:
- To give \( V_{out}\text{-low} \) while maintaining \( V_P \) and keeping it and M0 in saturation
Design for larger swing

You may want large swing for good SNR

But there are two constraints for large swing:

1. At least:
   - $V_x > V_p$ (swing limit on $V_x$)
   - But $V_p$ has to keep $M0$ in saturation

2. Better if: $V_x > (V_{DD} - V_{th})$
   - to keep $M1$ in saturation
     - To minimize $C_{gd'}$ (Miller effect) and maximize $R_D$ of $M1$

So, Max swing is

- $V_{DD} - V_p$-min = 1.55 V
  - Reaching the limit, usually can’t meet
- $V_{dd}$ to $(V_{dd} - V_{th}) = 0.5V$
  - For good performance
- $(V_{DD}$-Overdrive)/2 = 0.77V
  - Suggested typical

Also applies to the other direction of input
Design for smaller swing:

You want small swing for higher bandwidth

- Or less $I_{\text{tail}}$ for low power, smaller M0 size

Constraints:

1. Noise margin, SNR

2. Large M1 and M2 to get a high $V_P$

- To turn M2 off
- For example: $V_P > V_X - V_{\text{th}}$, if $V_X = 1.4\text{V}$, then $V_P > 0.9\text{V}$
- Large M1 and M2 is needed to get a $V_P = 0.9\text{V}$, this brings more load to previous stage

Suppose output swing from $V_X$ to $V_{DD}$
Another design example: EX2

- \( S \) and \( C \) \( \Rightarrow \) \( R = 1/(2.5 \times S \times C) = 800 \) ohm
- Tail current: \( (1.8 - 1.16)/R = 0.8 \) mA
- \( V_p > \text{Max (0.25, 0.4-0.5)} \)
  - Choose \( V_p = 0.25 \) V
- \( V_{bias} = V_{th} + 0.25 = 0.75 \) V
  - Leave 0.25 V as overdrive margin
- \( V_p \) and \( V_{bias} \) \( \Rightarrow \) \( W/L \) of \( M_0 = 48.6 \mu m/0.54 \mu m \)
  - Design \( M_0 \) to get such a tail current
- \( \text{IN}_{\text{high}} = 1.3 \) V, get \( W/L \) of \( M_1 \) to make sure \( V_p \) of 0.25 V \( \Rightarrow \) \( W/L = 4.32 \mu m/0.18 \mu m \)

Design specs example:
- Input swing range: 0.4/0.45 to 1.35/1.3
- Output swing range: 1.8 V to 1.16 V
- Data rate \( S = 5 \) G and Load \( C_L = 100 \) fF
- \( V_{th} = 0.5 \) V, \( V_{ov} = 0.25 \) V, \( L = 0.54 \) um for \( M_0 \)
Optimization and Verification: EX2

- If bandwidth allows, choose higher $R$
  - Results in more swing
  - Or allowing smaller $I_{\text{tail}}$

- If precise $V_{\text{bias}}$ and low gnd noise are available $\Rightarrow$ choose smaller overdrive margin $V_p$, to get more swing

- Check if M1 and M2 at saturation?
  - $\text{IN}_{\text{high}}-V_{\text{th}}=1.35-0.5=0.85 < \text{OUT}_{\text{low}}$ Yes, it’s good.

- Check if M1 or M2 is large enough to carry $I_{\text{tail}}$ when Input is high.
  - Requires: $(\text{IN}_{\text{high}}-V_{p}-V_{\text{th}})^2 W_{M1}/L_{M1} > (V_{\text{bias}}-V_{\text{th}})^2 W_{M0}/L_{M0}$
  - Right=$(0.75-0.5)^2*48.6/0.54=5.6$
  - Left=$(1.3-0.25-0.5)^2*4.32/0.18=7.26 > \text{Left!}$
    - Left $> \text{Right}$, some margin is left for body effect
Easy Scaling

- To scale what?
  - To drive $N$ times capacitive load or to provide $N$ times bandwidth

- How to scale?
  - $R/N$
  - $M_0 N; M_1 N; M_2 N$

- Scaling effect
  - $I_{tail} N$
  - Bandwidth$N$ or equivalent cap load $N$
Resistor variation

- Resistors vary largely across corners than transistors

- When R increase
  - $V_p$ decrease
  - $I_{\text{tail}}$ remains or negligible decrease
  - Output swing increase
  - $I_{\text{tail}}$ need to be calibrated to compensate R variations
Resistor variation – cont.

Circuit for Project – Use Ideal OpAmp

- Assume $R_S$ and $R_L$ will vary at same direction linearly
- But since $V_{\text{bandgap}}$ remains same, $R_S I_0$ and $R_L I_2$ will remain constant, as well as output swing
Static Differential Receivers

Advantages:

- More sensitive
  - Determined by $gm$ of source coupled pair and $R\Delta$ of load
  - 20 – 100 mV
- Less input offset voltage
  - Determined by nFET, pFET mismatch
  - 10 mV
  - Can be compensated by trim transistors
- Rejects common mode noise at input (i.e. can reject part of received SSN and crosstalk)

FIGURE 4-59. DC Transfer Characteristics of a Source-Coupled Pair
**Design Issues:**

- **Differential voltage gain**
  \[ A_d = \frac{V_{out_P} - V_{out_N}}{V_{in_P} - V_{in_N}} \]
- **Output swing**
- **Common Mode Rejection Ratio**
  \[ CMRR = \frac{A_c}{A_d} \]
  CM gain: \[ A_c = \frac{V_{out_P} + V_{out_N}}{V_{in_P} + V_{in_N}} \]
- **Bandwidth**
Max Swing and Differential Gain

Maximum Swing (on one side)

\[ = I_{bias} R \text{ (as before)} \]

Differential gain:

Using Small Swing equivalent circuit

\[ |A_v| = g_m(R) \frac{1}{g_{ds}} \]

Assuming IV square law relationship (first order equations)

\[ \frac{\Delta I_D}{\Delta V_{in}} = A_{I,DM} = \sqrt{\beta I_{SS} R} \]

\[ A_v = A_I R \]

Note: Gain/BW tradeoff,
Since both change with R
Common Mode Gain:

\[ \frac{\Delta V_{out}}{\Delta V_{in}} = A_{v,CM} = \frac{-R_D / 2}{1/(2g_m) + R_{ss}} \]

- $R_{ss}$ is impedance of current source
- Good Common Mode Noise Rejection
Differential Loads

Converts output current into voltage

- Differential resistance
  \[ r_\Delta = \frac{\partial \Delta V}{\partial \Delta I} \]

- Common Mode resistance
  \[ r_C = \frac{\partial V_C}{\partial I_C} \]

- \(-ve\) \( R_\Delta \)
  \( \rightarrow \) Positive feedback
  \( \rightarrow \) Hysterisis

Any load mismatch
\( \rightarrow \) Reduction in Common Mode
Noise Reduction
(or mode couple \( V_C \rightarrow V_\Delta \))

Transistor loads increase \( C \)
and decrease BW

**TABLE 4-5 Impedance of Differential Loads**

<table>
<thead>
<tr>
<th>Load</th>
<th>( r_C )</th>
<th>( r_\Delta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>( R )</td>
<td>( R )</td>
</tr>
<tr>
<td>Current mirror</td>
<td>( 1/g_m )</td>
<td>( 1/\lambda I_1 )</td>
</tr>
<tr>
<td>Cross-coupled</td>
<td>( 1/g_m )</td>
<td>(-1/g_m )</td>
</tr>
<tr>
<td>Infinite impedance</td>
<td>( 1/2g_m )</td>
<td>( \infty )</td>
</tr>
</tbody>
</table>

**FIGURE 4-60. Some Differential Load Circuits**

(a) Differential Load
(b) Resistor
(c) Current Mirror
(d) Cross Coupled
(e) Infinite Impedance
Inductive Loads

Inductive load creates resonant load

- Permits higher frequency of operation and larger swing
- At expense of considerable added area for spiral inductor
Differential Latch

Choose this SCL M/S latch for high speed, differential, noise rejection

- High power consumption

**Design @ transistor level**

Bandwidth, $C_{\text{load}}$

$\Rightarrow$ Pull up Resistor

Swing $\Rightarrow$ Tail current

Swing and $V_{\text{th}}$ $\Rightarrow$ $V_p$

Design transistors’ $W/L$

Simulation with $C_{\text{load}}, C_{\text{wire}}$

Reduce power dissipation as long as requirements met
Standard SERDES Design

Standard Current Mode Structure:

\[ \text{Equalizer Driver} \quad \text{Equalizer Receiver} \quad \text{DFE} \quad \text{CDR} \]

\[ \text{N:2 Mux} \quad \text{2:1 Mux} \quad \text{Channel} \quad \text{clk} \]
CML Selector

2:1 MUX
Pre-Emphasis

Simple digital z-domain high pass filter
- Must ensure proper voltage swing

E.g. 2-tap FIR

\[ H(z) = a_0 + a_1 z^{-1} \]
\[ r = -\frac{a_1}{a_0} \]
\[ H(z) = a_0(1-rz^{-1}) \]
\[ H(w) = a_0(1-re^{jwt}) \]
\[ |H(\omega)| = a_0(1+r^2-2rcos(\omega t))^{0.5} \]
\[ |H(\omega=0)| = a_0(1-r) = a_0 + a_1 \]
\[ |H(\omega t=n\pi)| = a_0(1+r) = a_0 - a_1 \]

Boost = \( \frac{a_0-a_1}{a_0+a_1} = \frac{1+r}{1-r} \)

HPF if \( a_0 > 0 \), and \( a_1 < 0 \)
Current mode signaling in serial link design

Fixed Weights: Current Sources determined by transistor size
Programmable Weights: DAC current source
DAC current source

Programmable current source for adaptive equalization
**Tap Sizing**

First order design procedure for fixed weights:
If response at end of line to a 010 pulse is:

Then size of taps are \(-a_1\), \(-a_2\) and \(-a_3\) as given above
(i.e. Use taps to subtract this amount from previous “1”s if present).
RX Equalizers

Feed Forward Equalizer
- Usually analog
- Can equalize pre-cursor ISI as well as boost HF

Decision Feedback Equalizer
- Can equalize post-cursor ISI
- Easy to adapt (information at RX)
**DFE Equalization**

**DFE Block Diagram**

\[ y[n] = x[n] - w_1\hat{y}[n-1] - w_2\hat{y}[n-2] - w_3\hat{y}[n-3] \]

Loop Delay must be smaller than 1 UI

- Challenging
DFE Example Implementation

Input

2 bit feedback

Slicer
DFE Loop Unrolling

Speculation used to reduce critical path in DFE

\[
\hat{y}[n] = \begin{cases} 
  x[n] - w_1 & \text{if } y[n-1] = 1 \\
  x[n] + w_1 & \text{if } y[n-1] = -1 
\end{cases}
\]
Clock and Data Recovery (CDR)

Phase Lock Loop type...

- VCO generates clock
- Phase detector compares clock phase with input
- Output of phase detector used to advance/retard clock, via charge pump
- Filter used to ensure stability, and give good transient response
Output of phase detector: \[ x_m(t) = x_c(t) \cdot x_r(t) \]

VCO frequency: \[ \omega_r(t) = \omega_f + g_v y(t) \]

Where \( g_v \) is the sensitivity of the VCO expressed in Hz/V

VCO output:
\[ x_r(t) = A_r \cos\left(\int_0^t \omega_r \, d\tau\right) = A_r \cos(\omega_f t + \varphi(t)) \]

Where \( \varphi(t) = \int_0^t g_v y(t) \, d\tau \) is the input to the loop filter

Note: This analysis assumes a mixer, not phase detector
Basic Equations

Loop Filter:
Recieves $x_m(t) = \phi(t)$ as an input and has an output response

$$x_f(t) = F_{filter}(x_m(t))$$

Where $F_{filter}$ is the response of the filter. This is the input $y(t)$ to the VCO.

Small Signal Analysis
Input sinusoid $x_c = A_c \sin(\omega_c t)$
Output of PD

$$x_m = A_c \sin(\omega_c t) \cdot A_r \sin(\omega_r t + \phi(t)) = (A_c A_r/2) \sin(\omega_c - \omega_r - \gamma \phi(t)) + (A_c A_r/2) \sin(\omega_c + \omega_r + \gamma(t))$$

At lock

$$\omega_c \approx \omega_f$$

Thus, input to VCO

$$y(t) = x_m(t) \approx A_c A_r \phi(t)/2$$

And the PLL is locked

Output of VCO
Rejected by loop filter (high frequency)
Open Loop Gain

\[ \frac{\theta_o}{\theta_i} = K_p K_v F(s) \]

ie. Output Phase / Input Phase = Phase detector gain (phase/rad) * Filter Gain (Fs) * VCO gain (phase/rad)

- Requirement: Be Stable
- E.g. Bode plot stability requirement
Loop Stability

Bode Plot

- Unity gain and > -180° phase shift needed for oscillation
  - But not at same time
  - Margin defines stability
Closed Loop Gain

\[
\frac{\theta_o}{\theta_i} = \frac{K_p K_v F(s)}{s + K_p K_v F(s)}
\]

If filter = simple RC low-pass (one pole) filter

\[
F_s = \frac{1}{1 + sRC}
\]
Loop Response

Loop Response becomes

\[
\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + s / RC + \frac{K_p K_v}{RC}}
\]

Denominator takes form

\[
s^2 + 2s\zeta\omega_n + \omega_n^2
\]

Where \(\omega_n = \sqrt{\frac{K_p K_v}{RC}}\) is the natural frequency of loop convergence on phase

Want fast for fast lock

And \(\zeta = \frac{1}{2\sqrt{K_p K_v RC}}\) is the damping factor

Want critical (0.707) for fast lock

Note: First order loop does not permit independent control of \(\omega_n\) and \(\zeta\)
**Second Order Loop Filter**

More effective filter is to use lag-lead filter

\[ F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)} \]

Which has two time constants

\[ \tau_1 = C(R_1 + R_2) \]
\[ \tau_2 = CR_2 \]

Now natural frequency and damping factor can be individually controlled

\[ \omega_n = \sqrt{\frac{KpKv}{t_1}} \]
\[ \zeta = \frac{1}{2} \omega_n t_1 + \frac{\omega_n t_2}{2} \]
XOR phase detector

Simplest phase detector

\[ \text{Average value of out} = \frac{\tau}{T} \]
Hogge Phase Detector

- Delay between Din and Ck compared against Tck/2

- Average of up and down not 0 until clock centered on data

Goes to Charge Pump

PDout_{av}

Delay between Din and Ck compared against Tck/2
Alexander (Bang-Bang) PD

- Rising edge samples Data (D)
- Falling edge samples Boundary (B)
- If $D_n \neq D_{n+1}$, and $B = D_{n+1}$, CK is late, increase Vcontrol of VCO
- If $D_N \neq D_{n0+1}$ and $B = D_n$, CK is early, decrease Vcontrol of VCO
- If $D_n = D_{n-1t}$ (no transition), do no change Vcontrol
Voltage vs. Current Mode Drivers

Voltage Mode

- Sends $\Delta V$ down line
- Advantages:
  - Larger swing
  - Less power in TX
- Disadvantages
  - Slower $\Delta t = C \Delta V/I$
  - More SSN
  - Complementary, not differential

Current Mode

- Sends $\Delta I$ down line
  - Converted to $\Delta V$ by termination resistors
- Advantages:
  - Faster
  - Less SSN
  - True differential
- Disadvantages
  - DC power
Basic Voltage Drivers

Techniques to prevent short-circuit current:

NAND: $tr > tf$
NOR: $tf > tr$
Use rise, fall times to prevent $I_{sc}$
(beware of process spread)

<table>
<thead>
<tr>
<th>En</th>
<th>Data</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>z</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>z</td>
</tr>
</tbody>
</table>

"break nMOS"
"make pMOS"
Rise Time Control

Goal: Reduce $di/dt$ without significant reduction in delay

- Typically $tr < 0.3 - 0.5 \ t_{bit}$
- Process, temperature variations $\Rightarrow$ Active control might be desirable (e.g. Use nMOS as pFET and control “resistance”)
- First stage to switch usually the largest
Output Impedance Control

e.g. To precisely match line in series termination

- Digitally trimmed circuit
- NC1, NC2, PC1, PC2 produced by comparing copies of the drive FETs with an off-chip resistor (e.g., voltage division or a bridge)
Voltage Mode Pre-emphasis

Tap weights effectively set by transistor sizes:
- $a_1$ tap smaller transistors than $a_0$ tap
Detection & Sampling

Eye requirements at input to RX:

- To meet requirements to sample and amplify signal in presence of noise, timing skew and jitter

\[ \text{skew+jitter} \quad \text{aperture time} = t_{\text{setup}} + t_{\text{hold}} - t_r \]

Why? aperture time = \( t_{\text{setup}} + t_{\text{hold}} - t_r \)

As \( t_{\text{setup}}, t_{\text{hold}} \) measured to 50% points, aperture at top & bottom of eye (at 10%, 90% points)
On-chip Termination

Binary-weighted trim resistors

- Set trim bits through comparison of a reference circuit with an off-chip resistor
  - Bridge circuit for comparison
  - Use same values for r0, r1, r2 for actual RX terminations
  - Tgate configuration gives linearity over wider range

![Diagram of on-chip termination circuit](image)
FET Resistors

Can give better predictability than Polysilicon resistors:

FIGURE 4-61. FET Resistors

(a) Triode  (b) Two-Element  (c) Pass-Gate
(Composite: Diode connected on RHS)

FIGURE 4-62. I-V Characteristic of Two-Element FET Resistor
**ESD Protection**

Static electricity caused by human and machine handling of ICs

- **Human body model:**

  ![Diagram](image)

- **Effects of ESD**
  - Breakdown of gate oxide (at $7 \times 10^8$ V/m)
    - “First breakdown” (not necessarily destructive)
    - 4.9 V for 7 nm thick gate oxide
    - 350 V for 0.5 μm thick field oxide
  - Thermal runaway due to high IDS
    - “second breakdown” (destructive)
  - Avalanche and Zener breakdown in parasitic diode
**ESD Protection Circuits**

**Overall structure**

- **Primary shunt**
  - Goal: to drain current to neighboring input pad through ESD supply
  - Use parasitic diode, FET (using field oxide) or bipolar transistor
- **R**: Low-pass filter. Can be an L, at expense of increased area
  - Use poly or diffusion resistor
- **Secondary shunt**
  - Goal: Voltage clamping: diode-connected nFET

- **Note**: Adds ~1 pF of capacitance to input
Summary Questions

What determines the eye opening requirements at an un-equalized RX?

- Horizontal
- Vertical

What are the advantages of DM circuits over single-sided circuits?

How are terminations matched to the line?
Summary Questions

What are the tradeoffs in DM TX design?

What are the tradeoffs in DM RX design?

What is one method to size the taps in a FFE TX DSP?
Summary Questions

What is the function of the loop filter in the PLL?

How do you optimize the loop filter response?