4. *Dynamic Combinational Circuits*

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Outline

1. Dynamic Gate Basics
2. Domino Logic Styles
3. Dual Rail Domino
4. Bootstrap circuit

References

- Dally & Poulton, Chapters 4, 12.1
- Kang and Leblici, Chapter 9
- Bernstein, Ch. 3
- Gu, Sharaf, et.al. Ch. 4
Objectives and Motivation

Objectives:

- Understand approach used in designing a variety of dynamic logic circuits
- Understand advantages and disadvantages of different topologies

Motivation

- Dynamic logic circuits are important for high speed design. This provides an in-depth treatment
Dynamic Logic Gates

Basic Dynamic NAND gate:
- Clock = Low : Precharge S
- Clock = High : Evaluate pull down chain
- Low CL  ➔ Fast

Potential Problems
- Can this gate drive another similar gate?

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Dynamic Logic Gates

... Potential Problems:

- **Charge Sharing.** If A → 1 after clock goes Hi, while B is 0, then voltage at node S1 reduced.

- **Capacitive Coupling.** Even with A=B=0, parasitic noise coupled to node S1 or S2 can bring those nodes down. E.g. Crossing metal trace transitioning from 1- > 0

- **Charge Leakage.** If clock stops stored ‘1’ at S1, S2 will leak away

Solution?

**Potential Problem:**

- **Keeper:** Restores logic-1 while clock hi if A or B=0.

- **Inverter:** Ensures rising outputs only while clock hi

+ ensure A can only RISE After clock → 1
**Better Dynamic Logic Gates**

**Solution:**
- Disable keeper during evaluate
- Ensure inputs only RISE when clock=1 to prevent charge sharing

**How to minimize Ithru?**
Impact of $W_p/W_n$

- Large $W_p/W_n$ → More susceptible to noise on $S$
- Large $W_p/W_n$ → $Out$ rises sooner and $p2$ turns off sooner
Other Solutions

Tradeoff area for better control of p2:

Keeper “pulsed” on - Not fighting Pull downs

BUT: Dynamic nodes still unprotected for part of clock cycle
Transistor Sizing in Dynamic Logic

Want graded sizing for fastest transient operation:

\[ \text{Delay} \propto R3 (C1 + C2 + C3) + R2 (C1 + C2) + R1 C1 \]
Domino Logic

Satisfies requirement of rising inputs only

During evaluation A, C, E can only fall; B, D, F can only rise.

- Rules:
  - Previous stage can only drive top nFET in following stage
  - Pull-down clock nFETs can be eliminated in follow-on stages
Domino Logic

Transistor Size tradeoffs:

- **Keeper (p2)**
  - Wider (stronger) → better NMH at I1
  - Narrow (weaker) → faster + lower power
  - $W_{\text{keeper}} \sim W_N/4$ typical

- **Inverter (n4, p3)**
  - Larger → faster
  - $W_p > W_n$ → Increases NML @I1 → Better noise immunity at A inputs
    - Reduces time p2 on, and thus p2 load on n1-n3

- **Pull-down chain**
  - $W_n3 > W_n2 > W_n1$ to maximize $t_{\text{fall}}$

- **Precharge**
  - $W_p1$ determines pull-up time
Dual-Rail Domino

Many logic functions can not achieve glitch-free operation

- E.g. Arithmetic (consider carry chain)
- Solution: Dual-rail logic
  - Produce signal and signal’
- Actually:
  - Differential ckt with precharge added
  - Desire weak pfet pullups

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\[ a = a_0 = a_1' \]
\[ b = b_0 = b_1' \]
\[ c = c_0' = c_1 \]
Operation

Draw Waveform:

- **Clock**
  - Waveform

- **a1 = a0’**
  - Waveform

- **b1 = b0’**
  - Waveform

- **x0**
  - Waveform

- **x1**
  - Waveform

- **c1 = c0’**
  - Values: 0 1 0

FIGURE 4-45. A Dynamic Dual-Rail XOR Gate
**Dual Rail Domino**

**Size Tradeoffs:**

- **Half-latch**
  - $f = (A \cdot B)$
  - $f' = A \cdot B$
  - $B'$

- **Precharge** (size → $t_{rise}$)

- **Evaluate pFETs**
  - $W_n > W_p$ (fights half-latch)
  - $W_n$ increases towards bottom

- **Note:** Might buffer $f$ and $f'$ with INV to increase noise tolerance

- **Largest PD transistor:** $A > B, B' > A'$

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Other Variations

Dynamic Logic can lead to high density implementations of complex functions:

E.g.

Compound Logic

Multiple Output
**Domino Logic**

**Advantages:**
- Lower Cloads $\Rightarrow$ faster
- No crowbar current $\Rightarrow$ faster, lower noise generation

**Disadvantages:**
- High clock power
- Careful timing design of clock
- Difficult to diagnose timing fault in chip
- Lower noise immunity
  - DC margins:
    - Clock noise $< |V_t|$ to prevent both $p_1$ and $n_3$ being on at same time
    - $V_A$ and $V_B$ must stay $< V_t$ for input-low
  - AC margins can be higher
- Subject to charge sharing
Summary

What is the main advantage of dynamic circuits?

What are some of the disadvantages?

What is dual-rail domino used for?