ECE 733: Digital Electronics  
Spring 2011  

Course Overview & Policies

Class Schedule:  Monday, Wednesday, 5.20 – 8.40 EB2 1226

Instructor:  Professor Paul D. Franzon, Ph.D.
Office:  EGRC 443, (919) 515-7351
E-mail:  paulf@ncsu.edu
Home page:  www.ece.ncsu.edu/erl/faculty/paulf.html
Office Hours:  Some Mon and Wed 2.30 – 3.30, and some Mon, Wed or Fri 3.50 – 5.05 (EB2 2116).  See on-line schedule to determine which days I am holding office hours.

Course Objectives.  Provide an in depth study of selected topics in the design of digital CMOS and physical-circuit codesign of digital circuits, at the transistor level.  Topics will include CMOS scalability; high-speed logic design; chip-package codesign; and high-speed I/O design.

Course Outcomes
- Student will understand the impact of technology scaling and variability on circuit design
- Student will be able to describe the different types of high-speed circuit styles and how to design in them
- Student will be able to design a high-speed synchronous logic circuit to specifications
- Student will be able to describe how to design the different sub-circuits in memory blocks
- Students will be able to describe the factors that go into high-speed I/O design
- Students will be able to describe the different approaches to high-speed I/O design
- (On-campus only) Students will be review a topical paper in advanced CMOS design and present a synopsis of its key results
- (On-campus only) Students will have an understanding of issues in the design of emerging memories, ultra-low power design and chip-package co-design
- (On-campus only) Students will be able to conduct a system level design trade-off investigation of an I/O sub-block

Lab TA/Graders:  Announced on web site.

Class Schedule and Delivery Method (on-campus students):  A mixed mode of delivery will be used.  Students will be expected to review recorded lectures per a posted schedule.  The class will meet approximately once a week for the following purposes:
- To answer questions arising from the lectures
- To conduct exercises to reinforce learning material
- To conduct student lead discussions of key papers in emerging topics in CMOS digital circuit design
Most of these class meetings will be in the Wednesday slot.  Attendance is expected and will be recorded.

Communications:  Students are strongly encouraged to use the Bulletin Board for questions that are not considered “private”.  If the question is a good discussion topic, or one that a peer can answer, myself and the TAs might not specifically respond unless it is clear the discussion is not solving it.  However, if it is clear that the questions can only be answered by one of us, we will do so as soon as practical.  TA-manned Labs should be used for problems related to CAD tool and code debug issues.  Though I hold my on-campus office hours in a Lab, my priority will be solving student issues that can not be addressed by a TA.  For addressing issues that the above methods are not suited for, email is preferred over the telephone.

Labs.  Regular TA-manned labs will be established.  You will find these very useful for resolving design and tool questions and should be your primary method to do so.

Textbooks & Notes:
Purchase is optional:
References
Course notes, papers, project assignments, etc.: The wolfware course locker will be used to distribute course notes, papers, and assignments. Please make sure that you print the first set of notes before the first class from the website. Also note that the notes distributed on-line are NOT the complete notes for the class. Classroom attendance and note-taking is expected.

You will find the course website and bulletin board on wolfware, as linked from the page www.courses.ncsu.edu/ece733. I emailed the class last week. If you did NOT receive these emails, check your “official” email address at www.ncsu.edu “directories” in the top right corner.

Prerequisite: Grade of B or better in ECE 546 or equivalent. Functionally, I am assuming that students are familiar with the basics of MOSFET operation and MOSFET circuit design, e.g. linear and saturation modes, and the design and operation of CMOS static logic gates. I will assume that you also have access to, and know how to use, a suitable circuit simulator, such as Hspice, and know how to perform schematic capture and simulation within the NCSU Cadence environment.

Course Projects: In order to provide an in-depth experience, you will also carry out two small design projects. The projects are not finalized yet but are likely to be a high-speed CMOS flip-flop design, and a CMOS transceiver physical-logic co-design. An informal lab will be organized to provide active help for the projects and provide a forum for evaluation of the projects. Though lab attendance is not required, little assistance will be available outside of the labs.

Homework TurnIn
  o On-campus students. Unless specifically requested, please bring a paper copy to class.

Recorded Course Syllabus
  1. Introduction
  2. Flip-flops
  3. Timing and design
  4. Interconnect
  5. Transceiver Design
  6. Nanoscale circuits and architectures

Software Requirements. You will need access at least to a Spice simulator for this course, and preferably also a schematic capture tool. On campus students will be encouraged to use Hspice, and Composer. Off campus students will be given access to these tools but can also use their companies or third party tools (e.g. http://www.duncanamps.com/spicesim.html lists a number of free Spice tools).

Student Evaluation. Students will be evaluated as follows:
  ▪ Homeworks. There will be a small number of homeworks to force review of specific issues. (10%)
  ▪ Midterm. (10%)
  ▪ Projects. You will be individually graded on two small projects. Project 1 is worth 20% of the grade, and project 2 is worth 20%. (40%).
  ▪ Class Research Presentation. Each student will be required to present a synopsys of a research paper or area (15%).
  ▪ Essay. Each student will write an essay on nanoscale electronics (15%)
  ▪ Final Exam. There will be a 75 minute final exam.
  ▪ Due to the added material, there is NO FINAL

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<tr>
<th>Exam</th>
<th>Date</th>
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<tr>
<td>Midterm Exam</td>
<td>Wednesday, February 10</td>
<td>In class</td>
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<tr>
<td>Final Exam</td>
<td>Wednesday, May 4</td>
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Collaboration is encouraged on the homeworks and projects but you are expected to turn in individual solutions and reports. Sharing of electronic files is expressly forbidden. Collaboration on the detailed transistor design is
also forbidden. It is easy to tell if a circuit design has been copied. The exams will be open-book, open-notes, multiple-choice and short answer exams.

Instructor Research Interests
- Application specific processors. Current projects focus on applications and design of 3DICs.
- Interconnect, including transceivers, electronic packaging, on-chip interconnect, and between-chip interconnect.
- Nanocomputing – how to build the computers that will eventually displace or complement CMOS.

Students with disabilities
Reasonable accommodations will be made for students with verifiable disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653. [http://www.ncsu.edu/provost/offices/affirm_action/dss](http://www.ncsu.edu/provost/offices/affirm_action/dss) For more information on NC State's policy on working with students with disabilities, please see [http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html](http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html)

Academic integrity
All the provisions of the [code of academic integrity](http://www.ncsu.edu/provost/hat/current/appendix/appen_k.html) apply to this course. In addition, it is my understanding and expectation that your submission on any test or assignment means that you neither gave nor received unauthorized aid. For homeworks and projects, while collaboration is encouraged, sharing of design data is expressly not permitted. In particular sharing of any electronic files, or schematics is forbidden.