2. Static Combinational Circuits

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Outline

1. CMOS Inverter
   • DC and AC characteristics
2. Static logic gates
   • Structure
   • Relative transistor sizing
   • Multi-Vt circuits
3. Differential Cascode Voltage Switch (DCVS) Logic
   • Structure
   • Transistor Sizing
4. Pass Gate Logic
   • Structures & Alternatives
   • Transistor Sizing

References:

Dally & Poulton, Chapters 4, 12.1
Kang and Leblicici, Chapters 5, 6, 7
Sutherland, Sproull, Harris, “Logical Effort”
Objectives and Motivation

Module Objectives:

- Understanding of basic design principles and tradeoffs behind high-speed complementary logic gates
  - Revision
- Understanding of AC characteristics of static gate “amplifiers”
- Understanding of operation of DCVS and Pass Gate Logic
- Understanding of relative advantages and disadvantages of each logic family

Motivation

- Static gates used in numerous high-speed and low-power designs due to simplicity of design, and robustness
- Revision in these topic of issues relevant to flip-flop design
Basic CMOS Circuit Analysis

Core Principle:

Analysis of any digital circuit usually revolves around determining the transistor states for each region of operation.

Basic Approach: 1. Estimate states or voltages
2. Calculate voltages or states
3. Make sure self-consistent

<table>
<thead>
<tr>
<th>Region</th>
<th>State</th>
<th>Equivalent Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>V_{GS}</td>
<td>&lt;</td>
</tr>
<tr>
<td>$</td>
<td>V_{GS}-V_{T}</td>
<td>&gt; V_{DS} \geq 0$</td>
</tr>
<tr>
<td>$V_{DS} \geq</td>
<td>V_{GS}-V_{T}</td>
<td>\geq 0$</td>
</tr>
</tbody>
</table>

Source of “majority carriers”
(e- in nmos case, p+ in pmos)
CMOS Inverter

Static CMOS Inverter:

- **Transfer Characteristic:**

1. $V_{in} = 0$, $V_{out} = V_{dd}$
   - N: $V_{GS} = 0$, $V_{DS} = 3.3$, $|V_{GS}| < |V_T|$ : Off
   - P: $V_{GS} = 3.3$, $V_{DS} = 0$, $|V_{GS} - V_T| > V_{DS}$ : LINEAR

2. $V_{in} > |V_T|$
   - N: $V_{GS} \approx 1$, $V_{DS} \approx 3$, $V_{DS} \geq |V_{GS} - V_T|$ : SATN
   - P: $V_{GS} \approx 3$, $V_{DS} \approx 0.3$, $|V_{GS} - V_T| > V_{DS}$ : LINEAR

3. $V_{in} \approx V_{out}$
   - N: $V_{GS} \approx 1.6$, $V_{DS} \approx 1.6$, $V_{DS} \geq |V_{GS} - V_T|$ : SATN
   - P: $V_{GS} \approx 1.6$, $V_{DS} \approx 1.6$, $V_{DS} \geq |V_{GS} - V_T|$ : SATN

- **High Gain Region**

Gain = $\frac{4}{((V_{GS} - V_T)(\lambda_p + \lambda_n))}$
CMOS Inverter

“Trip” Voltage

- where \( V_{\text{out}} = 0.5 \times V_{DD} \)
  - Both nFET and pFET in saturation

\[
I_{DSn} = -I_{DSP} \\
\frac{\beta_n}{2}(V_{in} - V_{Tn})^2 = -\frac{\beta_p}{2}(V_{in} - V_{DD} - V_{Tp})^2 \\
V_{in} = \frac{V_{DD} + V_{tp} + V_{in} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}
\]

- If \( \beta_n = \beta_p \) and \( V_{tn} = -V_{tp} \), \( V_{in} = V_{DD}/2 \)  
  \( (1.65 \text{ V with parameters on prev. page}) \)

- What if \( k_n = 2k_p \), \( W_n/L_n = W_p/L_p \), \( V_{DD} = 3.3 \), \( V_{tn} = -V_{tp} = 0.5 \)?
CMOS Inverter

Trip voltage moves with W/L

• Would you expect VIL, etc. to move with W/L?

How would you design an inverting receiver where input high noise and low noise have approx. equal magnitudes, e.g. for RX at the end of a noisy wire?
Shifting Trip Voltage Vth

Complete:

\[ k_R = \frac{k_n}{k_p} \]

\[ V_{DD} = 5 \text{ V} \]
\[ V_{T0,n} = 1.0 \text{ V} \]
\[ V_{T0,p} = -1.0 \text{ V} \]

Figure 5.24  Voltage transfer characteristics of three CMOS inverters, with different nMOS-to-pMOS ratios.
Transient (Step) Response

Idealized Input: Unit step

\[ V_o \geq V_{DD} - V_{tn} \]

\( t = 0 \)

Vo < V_{DD} - V_{tn}

90% - 10% Fall Time

\[ C_L \frac{dV_o}{dt} + I_{DS} = 0 \]

\[ t_f = C_L \int_{V_{DD} - V_{in}}^{0.9V_{DD}} I_{DS\, (satn)} dV_o + \int_{0.9V_{DD}}^{V_{DD} - V_{in}} I_{DS\, (linear)} dV_o \]

\[ t_f \approx 4 \frac{C_L}{\beta_n V_{DD}} \]
**Constant Current Approximation**

Actual Input: Ramp
Step response vs. response to input with rise time = output fall time

\[
\tau = \frac{V_{DD}C_L}{I_{DSS}}
\]

\((I_{DSS} = Satn current)\)

See Poulton and Dally for “derivation”
Constant Current – Rise Time

Input rise time affects output delay:

\[ T_{PHL} \approx \tau (1-r) \]

\[ T_{PHL} \approx \tau^{0.5} \]

See D&P for derivation.
Inverter as Small Signal Amplifier

Can be used to restore small swing “logic” (e.g. input from lossy channel)

- Gain in high-gain region
  \[ \text{Gain} = \frac{4}{(V_{GS}-V_T)(\lambda_p+\lambda_n)} \]
  About 20-40 practically

- Note: Miller effect increases apparent input capacitance in high gain region

- Frequency Response:
  - \( \frac{dv_{out}}{dt} = \frac{i}{C} = g_m v_{in}/C \)
    \( = \frac{I_{DSS}}{V_{DD}} v_{in}/C \)
  - Sinusoid: \( v_{out} = \sin \omega t = A \ v_{in} \)
    \( \Rightarrow dv_{out}/dt = \omega \sin \omega t \)
    \( \Rightarrow \text{When } A=1: \omega_1 = \frac{I_{DSS}}{V_{DD}}C = 1/\tau \)
    \( \Rightarrow \text{i.e. } f_1 = 1/(2\pi \tau) \)

\( f_1 \) called Gain-Bandwidth Product
Miller Effect Capacitance

Affects capacitance seen by small-signal equivalent circuit.

Miller's Theorem:

Series capacitance in gain ckt:

\[
\begin{align*}
&\text{Vin} \quad C_m \quad V_{out} = AVin
\end{align*}
\]

Can be transformed to the following equivalent circuit:

\[
\begin{align*}
&\text{Vin} \quad (1-A)C_m \quad AVin
\end{align*}
\]

A is -ve \( \Rightarrow \) Cin increases a lot in high gain region (at \( V_{inv} \))

\( \Rightarrow \) Zin = \( 1/j\omega \) Cin changes a lot in this region

\( \wedge \) Matters when constant known Zin matters
Static Logic Gates

Complementary pull-down and pull-up circuits

Analysis & Design Issues

- Body Effect changing Vtn for upper pull-up
- Transistor sizing:
  - Can speed up one path over another. (Note: Body effect on P2)
  - E.g. If path through ‘x’ is more critical, increase those transistors sizes.
  - If ‘y’ had to be faster (input arrived later in clock cycle) would it make sense to swap y with x?
Transistor Sizing in Pull Down Logic

Want graded sizing for fastest transient operation:

$\text{Delay} \propto R_3 (C_1 + C_2 + C_3) + R_2 (C_1 + C_2) + R_1 C_1$
Transistor Sizing

Key Steps:

- Simplify circuit as RC equivalent
- Consider RC delay from when transistor turns on
- Make sure to include any effects of delay opposing transistor turn-off

\[ \begin{align*} &x, y \to 1,1 \\
&x, y \to 0,1 \\
&x, y \to 1,0 \\
\Rightarrow n2 & \quad n1 \\
\Rightarrow p2 & \quad p1 \end{align*} \]
Static Complementary CMOS Logic

Advantages:
- Low power
  - Only leakage when not switching
- High Noise Tolerance
- No clock needed
- Good target for automatic synthesis

Disadvantages:
- High fan-out load (lower speed)
  - pFET and nFET loads
- High noise generation (crowbar currents and \( I_{\text{noise}} = C\frac{dv}{dt} \))
- Delay scales poorly with logical width
  - E.g. Multi-bit OR & NOR (e.g. zero detect circuit) much slower in Static CMOS than in domino logic
Static Complementary CMOS Logic

Main Uses:

- Automatic synthesis
- Random logic with low logic widths
- Logic or buffers with large loads
  - Ratio drivers
  - Not as much need to upsize pFETs to get equal rise and fall delays
  - Easier to drive large loads in Static CMOS than other styles
  - Can have logic in earlier stages

1x 3x 9x
Reducing Static Power Consumption

Variable Threshold Design

2.A. By Adjusting Body Voltage

- \( V_{Bp} = V_{dd} \) (active)
- \( = 2 \times V_{dd} \) (standby)
- \( V_{Bn} = GND \) (active)
- \( = -V_{dd} \) (standby)

2.B. By using a multi-Vt process

High-Vt transistors at top and bottom block sub-threshold leakage path during standby operation
Biasing $V_{BS}$ shifts device $V_T$ higher (for reverse bias) or lower (for forward bias). Here, 4V reverse bias yields 800mV higher NMOS $V_T$.

Forward bias (FB) increases subthreshold current due to junction leakage.

Interesting note – PMOS reverse bias (RB) $V_T$ shift is limited for some reason, saturates at 300mV shift at 1.5V FB – *impacts ability to use PMOS $V_{BS}$ to modify circuit properties*. 
DCVS Logic

Differential Cascode Voltage Switch Logic

- nFETs form differential (complementary) evaluate tree – pFET half-latch pull-ups
DCVS Logic

Advantages:
- Low fanout load
  - Faster speed, and lower \( I_{\text{noise}} = C \frac{dV}{dt} \)
  - Good noise immunity (hysteresis in latch, static)
  - No clocks
- Implicit inverse available (can save logic)
- Can have better logic density

Disadvantages:
- pFET fights pull-down chain
  - Higher crowbar current
- Higher device count in some applications

Found to be particularly useful in applications like ECC that benefit from rich XOR, XNOR trees

High-speed on-chip ECC for synergistic fault-tolerance memory chips
Fifield, J.A.; Stapper, C.H.;
Solid-State Circuits, IEEE Journal of
DCVS logic

Transistor Size tradeoffs:

- In general:
  - Want $W_n \geq W_p$, so can overcome pFETs
  - $(A, B) : (1, 0) \rightarrow (1, 1)$ or $(0, 0) \rightarrow (1, 1)$
    - Want $W_{n2} > W_{n1}$ so $n2$ can discharge $CL$ @ $f'$ quickly
- With transistor sizes shown here, there is a case for increasing the size of $p2$
  - Has to drive larger Drain/Source load
- Have to balance against $CL$ on previous stage
Transmission Gates

Pass Gates:

• What is the limitation of an n-type pass gate?

• Fix with a transmission gate:

Use for:

• Logic, esp. muxes
• Bi-directional structures
  • E.g. Segmented buses
Pass Gate Logic

Multiplexor:

\[ f = AS' + BS = S \lor B : A \]

What does the following do?

When is the only time you would use it?
Delay in Pass Logic

Regions of operation:

Vin=Vdd

0

Vdd

Vdd-Vtn

|VGS| < |VT| OFF
|VGS-VT| > VDS ≥ 0 LINEAR
VDS ≥ |VGS-VT| ≥ 0 SATURATION

RC delay model appropriate
Complementary Pass Logic

Save area on Transmission Gate or other fully complementary style by using an nMOS pass gate instead of Transmission Gate

- Low power (low switched capacitance)
- Restore using an inverter
- Prefer low-Vt nMOS transistor
- Compromises noise margin
  - Note: Pfet in INV only weakly turned off

\[
\begin{align*}
A & \quad B \\
\quad B' \\
A' & \quad B
\end{align*}
\]

\[f = (A'.B)\]

\[f'\] fully specified for all values of A, B (i.e., inverter input never floating.)
CPL

Advantages

- Low power
- Good speed
- Low area

Disadvantages

- Poor fan-in (i.e. can not have high number of inputs)
  - One pass gate in input chain best, two acceptable, more gets too slow (high internal RC)
- Poor drive strength
  - Limited by inverter
- Body Effect
- Reduced Noise Immunity
DCVS with Pass Gate

Advantages

- Does not have pFET sensitivity of DCVS
  - PG logic pulls UP as well as down
- Reduced device count over conventional DCVS or static
- Good noise immunity

\[ f = A \land B \]
Double Pass Transistor Logic

- Provides improved noise margin through incorporation of pFETs
- At cost of increased area
Swing Restored Pass Gate Logic

Add pull-downs
- Creates cross-coupled latch

Advantages:
- Improves noise tolerance
- Improves speed due to latch amplifier

Disadvantages
- Cross-over current during switching
- Limited output drive (still)
Explanation of thru-current

Swing restored PGL
A,B = 1,1

Thru-current until RHS transition finishes.

A: 1 → 0
Energy Optimized Pass Transistor Logic (EEPL)

Energy Economized
Swing restored PGL
A,B = 1,1

Added pFETs break current through path

A: 1 → 0

Vdd-Vt → 1
Complementary Pass Gate Logic

Advantages:
- High speed
- Low power
- Esp. In low-Vt process

Disadvantages
- Body effect
- Limited fan-in
- Reduced noise margin

Main Uses:
- Usually faster Muxes, byte aligners, barrel shifters than other logic styles
- Low-power arithmetic circuits
Fig. 3. CPL circuit modules. (a) Two-way logic. (b) Three-way logic.
\[ ... \text{CPL} \]

### Table III

<table>
<thead>
<tr>
<th>Parameters (Vdd=3.3 V)</th>
<th>Static</th>
<th>CPL</th>
<th>DPL</th>
<th>Dual Rail Domino</th>
<th>Single Rail Domino</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power @ 100 MHz</td>
<td>34.3</td>
<td>34.5</td>
<td>27.5</td>
<td>82.5</td>
<td>60.2</td>
<td>mW</td>
</tr>
<tr>
<td>Percentage</td>
<td>125</td>
<td>125</td>
<td>100</td>
<td>300</td>
<td>219</td>
<td>%</td>
</tr>
<tr>
<td>Delay of critical path</td>
<td>2.33</td>
<td>2.24</td>
<td>1.98</td>
<td>1.78</td>
<td>1.64</td>
<td>ns</td>
</tr>
<tr>
<td>Percentage</td>
<td>142</td>
<td>137</td>
<td>121</td>
<td>109</td>
<td>100</td>
<td>%</td>
</tr>
<tr>
<td>Energy @ 100 MHz</td>
<td>79.9</td>
<td>77.3</td>
<td>54.5</td>
<td>146.9</td>
<td>98.7</td>
<td>pJ</td>
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<tr>
<td>Percentage</td>
<td>147</td>
<td>142</td>
<td>100</td>
<td>270</td>
<td>181</td>
<td>%</td>
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<tr>
<td>Area: pMOSFET width</td>
<td>17700</td>
<td>8295.6</td>
<td>11935.5</td>
<td>14716.4</td>
<td>12064.4</td>
<td>(\mu\text{m})</td>
</tr>
<tr>
<td>nMOSFET width</td>
<td>9655</td>
<td>9141.5</td>
<td>7181</td>
<td>17728</td>
<td>14862</td>
<td>(\mu\text{m})</td>
</tr>
<tr>
<td>total tr. width</td>
<td>27355</td>
<td>17437.1</td>
<td>19116.5</td>
<td>32444.4</td>
<td>26926.4</td>
<td>(\mu\text{m})</td>
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<tr>
<td>Percentage</td>
<td>157</td>
<td>100</td>
<td>110</td>
<td>186</td>
<td>154</td>
<td>%</td>
</tr>
</tbody>
</table>

Low-power design techniques for high-performance CMOS adders
Uming Ko; Balsara, T.; Wai Lee;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 3, Issue 2, June 1995 Page(s):327 - 333
Summary

What 2 performance figures does the saturated DS current, IDSS, of a transistor determine?

In a gate pull down chain, how might the transistors be sized?

![Diagram of gate pull down chain]

How are multi-Vt processes used?
Summary

What is the main potential advantage of DCVS?

What is the main potential advantage of Pass Transistor Logic?