Latches and Flip-Flops

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Outline

• Design Goals
• Basic Latches and Flip-flops
• Optimizing Timing
• Single Sided Designs
• Differential Designs
• Some comparisons

References

• Dally & Poulton, Chapters 4, 12.1
• Kang & Leblecici, Chs 8-9
• Bernstein, Ch. 5
Objectives and Motivation

Objectives:
- Understand design goals and tradeoffs in flip-flops and how they are measured
- Be able to describe operation of a wide range of flips and recognize how the roles of individual transistors determine operation

Motivation
- Most complex high-speed digital circuit
- Constrains performance of logic and I/O
D-Latch:
- level-sensitive
- Tracks data while clock high
- Stores data while clock low

D-Flip-flop
- edge-sensitive
- Stores data on clock edge
Edge-Triggered Flip-Flops

Created from latches:
Two styles:

- Master-Slave Latch
- Pulse-Triggered Latch

[Diagrams showing two latch styles]
Goals of Flip-Flop Design

Timing and Clock Speed:

\[ t_{\text{clock}} \geq t_{\text{ck-Q-max}} + t_{\text{logic-max}} + t_{\text{setup}} + t_{\text{skew-max}} \]

Goal:
- Minimize \( t_{\text{DQ}} = t_{\text{Ck-Q}} + t_{\text{setup}} \)
Timing Closure:

- Ability to withstand max-min process and temperature variations depends on how much of the clock-period is taken up by setup and hold times

Goal:

- Constrains maximum \( t_{\text{aperture}} = t_{\text{setup}} + t_{\text{hold}} \)
Goals of Flip-Flop Design

Timing Related:
- Be able to drive good loads
  - Typical fan-out: 2-8 FO4 inputs
- Minimum susceptibility to clock slope (edge rate)
  - Most FFs have an max rise/fall time specification

Desirable to be able to incorporate logic into the flip-flop
Goals of Flip-Flop Design

Power Related

- Minimize internal power
- Minimize clock load
- Note: Speed-power tradeoff
  - Can design to minimize Power.Delay or Energy.Delay Product
  - Measured in fJ – gives minimum energy per transition (and energy-delay product for constant fclock)

Bit Error Rate Related

- Minimize susceptibility to:
  - Noise on clocks or signals (e.g. due to crosstalk)
  - Clock edge rate variations
  - Charge-sharing failures
  - Charge leakage failures, including alpha particle strikes
  - Power & ground noise

Other

- Facilitate test and debug (Be static & scannable)
Flip-Flop Basics

Generic Flip-Flop:

Sampling Stage:
- Must ensure input is sampled for both high and low D
- Fastest if no DC path from Vdd to Gnd during sampling

Output Stage:
- Drives load without disrupting stored state
Basic Bistable Static Storage Element

Cross-coupled inverter pair

Inverter loaded with itself:
• Regenerative feedback

Qualitative View:
Energy

Stable operating point
Unstable (high gain)
Stable operating point
Noise Margin

Add noise at one input:

\[ V_2 \ 
\]

\[ V_1 \]

Assume nominal \( V_2 = 1 \)

Small \( V_n \)

High gain \( \rightarrow \) no longer stable

Size of "boxes" determine NMs

Unity gain

Large \( V_n \)
Basic Latches

To store a logic level (change state):
- Must overcome the potential “hill” between two stable states

Some Methods:
- Use Transmission gates to break feedback path
  - D-latch
- Break supply current path (RS latch)
  - Reset/Set
  - D latch:

Can replace INV with logic

NOR RS latch
Other Methods To Change State:

- Directly over-powering regenerative feedback in storage cell
- Must generate a “negative noise margin” by the write (clk=high)
- In this case
  - \((W_1,W_2,W_4,W_6)>(W_3,W_4)>(P_1,P_2)\)
Quiz

What timing parameter are we trying to minimize in a flip-flop?

What are the two ways to overpower the natural stability of cross-coupled inverters?

tDQ=tCk-Q + tsetup
**Timing**

Tradeoff between $t_{\text{clock-Q}}$ and $t_{SU} / \text{thold}$:

Why?

Smaller $t_{SU}$ $\Rightarrow$ $\Delta V_x$ smaller

-Amplification Voltage growth exponential with time

$V_Q \propto e^{-t/\tau}$

$\Rightarrow$ Amplifier delay increases exponentially with decreasing $t_{SU}$ (I.E. with smaller $\Delta V_x$)

$Q$ “metastable” during amplification
Doing this in Project

Illustrate for D: $0 \rightarrow 1$ transition:

Conservative $t_{su}$:  \hspace{1cm} Aggressive $t_{su}$:  \hspace{1cm} Failure:

Clock \hspace{2cm} Clock \hspace{2cm} Clock

$D$ \hspace{2cm} $D$ \hspace{2cm} $D$

$Q$ \hspace{2cm} $Q$ \hspace{2cm} $Q$

$t_{su}$ $t_{ck-Q}$ \hspace{1cm} $t_{su}$ $t_{ck-Q}$ \hspace{1cm} $<t_{su}$

$\rightarrow$ One point on curve on previous page \hspace{1cm} $\rightarrow$ Another point \hspace{1cm} $\rightarrow$ Failure!

Reminder: Goal most likely to minimize $t_{DQ}$, not $t_{su}$
… Project Characterization

T_hold

Failure:

\[ C_k \geq t_{\text{hold}} \]

\[ D \]

\[ Q \]

\[ < t_{\text{hold}} \]

\[ \Rightarrow \text{Failure! NOT a valid } t_{\text{hold}} \]

Good:

\[ C_k \geq t_{\text{hold}} \]

\[ D \]

\[ Q \]

\[ \geq t_{\text{hold}} \]

\[ \Rightarrow \text{Good! (NO change in } Q \text{ due to } D) \]

\[ \geq t_{\text{hold}} \]
Timing

Objective: Minimize $t_{D-Q} = t_{SU} + t_{\text{clock-Q}}$

Often results in negative setup time

e.g. “strong-ARM flip-flop”
Other Timing Parameters

Hold period:

![Diagram showing hold period with no transitions allowed]
Other Timing Parameters

Effect of clock edge rate

- Flip-flop timing can be sensitive to clock edge rate (slope)
  - Can cause race-through in Master-Slave
  - e.g. pass-gate FF:

```
clk

clk'

T2 open

T1 open

Problem if T2 open longer than $T_{inv-delay}$ past this time
```
Latches Flip-Flops Characterized

Single-Sided
- C2MOS
- TSPC
- Transmission Gate

Double-Sided (complementary or differential)
- DCVS
- Single Transistor Clock
- Hybrid Latch Flip-flop
- Semi Dynamic Flip-flop
- Sense Amp Flip Flop
- K6 Flip Flop

Comparisons
**Common Questions**

How is the signal sampled on the clock 0 → 1 transition?

What determines:
- $t_{setup}$?
- $t_{thold}$?
- $t_{ck-Q}$?

How is the data stored?

What prevents false transitions from occurring when
- $D$ changes after $t_{thold}$?
- When clock goes low?
C2MOS Flip-Flop

Edge triggered Master-Slave device:

- Low power feedback
- Locally generated second phase
- Poor driving capability
- Robustness to clock slope
C2MOS Operation

Track (ck = 0)

Track (ck → 1)

"Holding" sampled value

Sampling input

=on
Timing Questions

1. What determines $t_{su}$ and $t_{hold}$?

2. What determines $t_{ck-Q}$?
**True Single Phase Clocked (TSPC) Latches & Flip-Flops**

Based on the following dynamic latches:

- Transparent while clock high:
  - When clock low:

Note: Only clock is needed, not clock’ or a second clock phase

- True single phase ➔ lowest skew in distribution

Make latches and flip-flops by mixing stages.

(Source: Yuang and Svenson)
TSPC Flip Flops

Example:
- Positive edge triggered static-input flip flop
  - SP + SP + SN + SN

- Observation:
  - SP stage simply inverts a while clk lo
  - Not needed if Q’ OK..
- Note, nodes a, b, Q’ float for part of clock period
  - Watch for inadvertant charge sharing
- Note can put logic in PU and PD chains
Operation – $D=0$

D=0, clk=0

$D \rightarrow 1$, clk $\rightarrow 1$

Note: $a/b$ floats high or low ($x0$, $x1$)

D$\rightarrow 1$, clk=1 ($Q'$ should not change)
Operation – $D=1$

$D=1$, $clk=0$

$D \rightarrow 0$, $clk=1$ ($Q'$ should not change)

Note: $a/b$ floats high or low ($x0$, $x1$)
**TSPC Issues**

**Timing:**
- tclock-Q is very quick
  - Must have logic between stages to prevent hold violation
- Can be sensitive to clock slope (next page)
- Has floating nodes during evaluate
- Very high clock load
Clock Slope

Example: Sensitivity of TSPC flip-flop:

Possible failure:

- $D$ remains high
- $a$ low when clock low
- $Q'$

Possible Fixes:

Reduce $W_{n1}$; enforce clock slope rules
Transmission Gate Master-Slave

PowerPC 603
- Clock Load
  - High
- Power
  - Low
  - Low power feedback
- Positive setup

- TG delay determines $t_{su}$
- INV(s) + TG gate determines $t_{ck-Q}$ (first INV only matters if $tsu$ very small)

$Q$ buffer makes timing less sensitive to load variations
### Differential (Complementary) Latches and Flip Flops

i.e. Requires both D and D’

### Conventional Latches and Master-Slave Designs
- DCVS
- True Single Phase Clocked Latch
- DSTC and SSTC

### Pulse-triggered Latches:
- HLFF
- DSFF
- SAFF
- ETL
**Differential Cascode Voltage Switch**

**Variants:**
- Static RAM style Latch
  - Operation explained earlier
  - Transparent when clk hi

**Simple DCVS:**
- Latch or flip-flop?
- Dynamic or static?
- Susceptibility to charge sharing can be reduced by placing inverters on Q and Q'
**DCVS**

Combine to make Master-Slave Flip-flop

- Better than single-sided flip-flops
  - Fewer gates than C2MOS
  - Fully static storage
  - Smaller clock load
  - Complementary \(\Rightarrow\) faster operation
Operation

Clock = low:
- Master “turned on”
- One of n1 or n5 turned on

Clock $\rightarrow$ high
- n1 or n5 overpowers latch

After thold, what prevents a false transition?
- If D changes, can NOT result in the off n1 or n5 turning ON, as no PU path in master
- D changing can only result in the on transistor turning OFF: OK as latch has already stored new value
Operation

Ck=0; D=1
... Operation

$Ck \rightarrow 1; D=1$

Master

Slave

$Q=0$
Ck=1; D→0
(expect to see no transition)
**DCVS**

**Variant: Ratio insensitive Latch**

- Removes need to “overcome” X-coupled latch to change state
  - Especially hard to overcome nFETs in X-coupled inverters
- Reduces sensitivity to process variations

- p5, p4 ensures Vdd/Gnd path broken when changing stored state
- p3 ties the “on” p1 or p2 to Vdd when clock is low and latch is holding its outputs

*Example: ‘0’ held:*

- D has not changed: Vdd path
- D has changed: Vdd path
**Operation**

Ck=0; D=1

```
D -> Q
```

Ck→1; D=1

```
D' -> Q
```

P3 OFF allows latch state to change easily
**Operation**

Ck→0; D=1 (latch event)

Ck=0; D→0 (expect no change)

P3 ON means latch data is preserved
DCVS latch with pre-charge

Add pre-charge to increase speed:

- Simple Latched Dual Rail Domino structure:

`Dynamic D latch with pre-charge`

`D latch with merged logic`
Single Transistor Clocked MS latches

Yuan & Svensson ’97

- Small clock load; charge sharing issues

Min. sizes. Ensures static operation if D changes while clk high.
operation

Ck=0; D=1

Ck→1; D=1

DSTC

DSTC
\section*{Operation}

$Ck=1; D->0$

\begin{center}
\includegraphics{diagram.png}
\end{center}

DSTC
Operation

Ck=0; D=1

Ck→1; D=1

SSTC
... Operation

Ck=1; D → 0

SSTC
**Pulse-triggered Latch**

**Principle of Operation:**

Hybrid Latch Flip-Flop (HLFF) (AMD, K6, Portovi, 1996)

- **Clocked Transistors**

  - $X$ pre-charged (clock low)
  - Pulse samples $D$ onto $X$
Operation:
- Absorbs skew
- Fully static (retains Q)
- Negative setup
- Allows cycle stealing
- Can add logic
- thold c.f. tD-Q

Precharge (clock low)

Precharge (clock high)

Storage
Operation (\(D=1\))

Ck=0; D=1

What determines t\(_{su}\)?

What determines t\(_{D-Q}\)?

Ck→1; D=1

\(X\) precharged

= turning off

= turning on

\(Q=1\)

\(\bar{Q}\)
Operation after sampling $D=1$

Ck=1; X precharges

Ck=1; $D \rightarrow 0$

Latch on RHS isolated from inputs, $p3$ starts precharge on $X$, even if $D$ stays at 1
Operation, \( D=0 \)

Ck=0; D=0

\[ Ck \rightarrow 1; D=0 \]

\( X \) precharged high

What determines \( t_{su} \)?

What determines \( t_{D-Q} \)?

If \( D \) changes from 1->0 too late into clock pulse, \( X \) would be partially discharged. If \( p4 \) turns on for long enough, 0 will not be stored.

Note: \( n6, n5, n4 \) – latch

\( Q=0 \)

抄自 https://www.ece.ncsu.edu/erl/faculty/paulf.html
**Operation**

Ck=1; X precharges

Ck=1; D → 1

*n2 on → dip in X due to charge sharing*

*Weak p3 reduces dip*
HLFF Waveforms

charge share $X$ to nfet $n_1$

Weak $p_3$ pulling $X$ high
Semi-Dynamic Flip Flop

Sun UltraSparc, Klass, VLSI Circuits 98

- $D$
- $Clk$
- $Q$
- $\overline{Q}$

$Vdd$

- $n1$
- $n2$
- $n3$
- $n4$
- $n5$
- $p1$
- $p2$
Operation

"1"

INV1-2
INV1-2

Clk = low : X precharged to 1, N1 is ON
Clk \rightarrow hi : D=0 : X stays high, N1 on then off, Q pulled down; 0 stored
D=1 : N1 goes low, leaving N1 on. Pulls Q high

No P/G connection on LHS \rightarrow X latched low by X-coupled inverters

After thold if D \rightarrow 1 : N1 is off : No change

After thold if D \rightarrow 0 :
**Operation**

Ck=0; D=1

What determines $t_{su}$?

What determines $t_{D-Q}$?

Ck→1; D=1

Q=1
Operation

Ck=1; D → 0

D=1; Ck → 0
Operation

Ck=0; D=0

What determines $t_{su}$?

What determines $t_{D-Q}$?

Ck→1; D=0

Q=0

What determines $t_{su}$?
Operation

Ck=1; D $\rightarrow$ 1

Because top left nFET turned off, Q does not change

Ck $\rightarrow$ 0

Q=0
SDFF Timing Waveforms
Sense Amp Flip Flop

Matsui, et.al. 1994, DEC Alpha 21264; StrongArm

- First stage: Sense Amp
  - Precharged to Hi when clk=0
  - p2, p3:
  - n3, n4:
- Clk → 1
  - Diff Amp amplifies change in D
  - p2 or p3 turn on, latching value onto storage cell
  - S' or R' go low
- Role of N5
  - Keeps both INVs “grounded” even if D changes
- If D changes after thold
  - N5 reduces swing onto INVs
- Strength of N5?
- SR latch
- Ideal for low-swing inputs

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Operation

Ck=0; D=1

Ck→1; D=1
**Operation**

Ck=1; D→0

Ck→0; D=1

RS latch unaffected as $\overline{S}, \overline{R} = 1$
SAFF Timing

Ck→1

Once N3 is sufficiently off to prevent full transition but on enough to start one

N2 not on long enough to pull down node 1 enough to start turning N3 off.

Delay in SR latch

tsu
tforbidden

Tck-Q
Add $Clk$ transistors and tie common-gate as cross-coupled inv
Modified SAFF

- Karnough map transformation!
- Symmetric output
Modified SAFF

- Pulse generating stage is unchanged
- Improves speed bottleneck of RS latch.
- Symmetric (Q, Qb) waveforms
- Strong driver transistors
- Weak keeper transistors
**K6 ETL**

- ETL (Edge Triggered Latch) based on HLFF
- Converts static single ended input to dual rail dynamic logic (i.e. domino)
  - Self reset property
  - Increases dynamic power
- Fast
- Small clock load
Operation

Clock Low:

Clock $\rightarrow$ Hi
Flip Flop Comparison

Test bench

- Total power consumed
  - internal power
  - data power
  - clock power

- Measured for four cases
  - no activity (0000… and 1111…)
  - maximum activity (0101010..)
  - average activity (random sequence)

Delay is (minimum $D-Q$) $Clk-Q +$ setup time
ECE 733 Class Notes

K6

Sense Amp

StrongArm

DSTC

SSTC

SDFF
Delay Comparison

- Pulsed design brings the fastest structures
Power Delay Product

- Real signals have the activity between 0 and 0.5 (■).
- Precharged hybrid structures are the fastest but their power consumption strongly depends on the probability of “ones”.
- More “ones” above the ■ point.
Clock Power Consumption

- DSTC MS latch
- SSTC MS latch
- K6 ETL
- StrongArm FF
- SA-F/F
- $mC^2$ MOS
- PowerPC MS latch
- SDFF
- HLFF

Local Clock power consumption [μW]
General Characteristics

- 60ps = FO4 delay in .2u technology
- min gate width 1.6u

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<th>Total transistor width [u]</th>
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Reduced Clock Swing FlipFlop

Goal: Reduce clock power

- Clock 20% - 40% of overall chip power
  - Sakurai (JSSC, 1998)
  - Same as SAFF
  - Pre-charge transistor well is tied to $V_{WELL} > V_{DD}$
    - $V_{TP}$ threshold voltage is increased
    - Low swing clock can turn P precharge transistors off
Low Swing Double-Edge Triggered Flip-Flop

- Kang (JSSC May 2002)
Flip Flop Design – Summary

In high performance circuits, what are some of the goals of Flip-Flop design?

What design characteristics tend to produce the best flip-flops?