Low Power Design

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Outline
1. Power consumption in CMOS
2. Strategies to reduce power consumption

References
• Rabae, “Low Power Design Essentials”
Minimizing Power Consumption

Power consumption in a CMOS module:

\[ \text{Power} = \sum N_{\text{switch}} f V_{dd}^2 C_{\text{load}} + \text{leakage power} \]

Dynamic Power  Static Power

- Sum over all nodes in circuit
- \( f \) = clock frequency
- \( N_{\text{switch}} \) = average % of clock periods in which node toggles (I.e. 010 or 101)
- \( C_{\text{load}} \) = capacitance of node

\( N_{\text{switch}} \)

- Clock: 100%
- Maximum for glitch-free logic: 50%
- Logic typically has \( N_{\text{switch}} \sim 0.1 \).
Minimizing Energy

Energy = \int \text{Power}.dt

Energy consumption in a CMOS module:

\begin{align*}
\text{Energy} &= \sum_{\text{cycles}} \sum_{\text{nodes}} N_{\text{switch}} V_{\text{dd}}^2 C_{\text{load}} + \text{leakage power} \\
&\times \text{time}
\end{align*}

- \( N_{\text{switch}} \) = average % of clock periods in which node toggles (I.e. 010 or 101)
- \( C_{\text{load}} \) = capacitance of node
Speed – Energy Tradeoff

Running at lowest possible voltage not always the best strategy

Optimum energy.delay (around 600 – 800mV)
Approaches seen so far in ECE 520 and 733

- Dynamic Voltage and Frequency Scaling
- Multiple Voltage Design
- Multiple threshold design
- Clock Gating
- Ultra-low voltage operation
- Low swing interfaces
- Resonant Clocks
- Double clocked circuits
- Low activity design
- Low voltage memories
- Reduced interconnect algorithms and technologies

Issues:
- Design Complexity
- Increased PVT impact at low supply voltages
- Noise
Multi-Vdd and Multiple Vt

Case Study: ALU for 64-bit Microprocessor

Using Multiple Thresholds
- Cell-by-cell $V_{TH}$ assignment (not at block level)
- Achieves all-low $V_{TH}$ performance with substantial reduction in leakage

[Ref: Y. Shimazaki, ISSCC'03]
[Ref: S. Dato, SLPE'94]
Algorithm Choice Matters

e.g. Ripple Carry Adder is the most power efficient but if you need a faster adder, there are better algorithms than Radix-2 Carry Look Ahead

[Diagram showing energy versus delay for different adder algorithms: R2, R4 CLA, R2 Ling, R4 Ling.]

- Conventional CLA: Higher stack in first stage, simple sum precompute
- Ling CLA: Lower stack in first stage, complex sum precompute, higher speed

[Ref: R. Zlatanovici, ESSCIRC03]
**Interconnect Power**

![Communication Dominant Part of Power Budget](image1)

- **Traditional Level Converter**
  - Requires two discrete voltage levels
  - Asynchronous level conversion adds extra delay

![Avoiding Extra References](image2)

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Other Strategies

- Having the right number of bits and no more
- Minimizing memory usage, esp. of bigger off-chip memories
- Minimizing usage of non-volatile memories
- ASIC or FPGA accelerators
- ASIP

(Application Specific Instruction Processors)
**Multi-Vdd designs**

Moving slower circuits to lower Vdd reduces power “for free” but now we need level conversion

- BEST to do level conversion in clocked elements - robust

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**Level-Converting Flip-Flops (LCFFs)**

**Pulsed Half-Latch versus Master–Slave LCFFs**

- Smaller # of MOSFETs/clock loading
- Faster level conversion using half-latch structure
- Shorter D–Q path from pulsed circuit

[Ref: F. Ishihara, ISLPED'03]
Domino style level converter

- INV2 is placed near 9:1 MUX to increase noise immunity
- Level conversion is done by a domino 9:1 MUX

Used in Itanium